UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

Activity report a.a. 2018/2019

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INTRODUCTION

Nowadays the increasing growth of big data applications, high serial data rates communications and cloud computing requires high bandwidth wireline performances. The most common metal connections are the coppers type, but their signal's losing is strongly frequency dependent. The optical interconnections are affected too of the frequency losing but in a minor quantity, for this reason they transport wideband signal over long distance. The optical links are more popular for the high data rate and remote communications. However, the implementation of optical system has many challenges about the sensitivity, the power consumption and the thermal design power constrains of the package. In order to improve more the data rate, in the 2005 the optical communications were associated to coherent modulations that has the high advantage to improve the spectral efficiency of the data. Nowadays the most used technology in optical receiver circuits is the bipolar, due to the high BW and low noise that it can achieve, but the high costs and its poor linearity, that is a stringent condition for the coherent communication, push to find equivalent solutions in the CMOS technology. For that reason, Huawei has signed a contract with the University of Pavia to start a research work in order to study and realize a Transimpedance Amplifier (TIA) to receive the current from a photodiode of an optical link in CMOS technology. In this context, many research opportunities are evolved, in particular my PhD subject is focused on an optical receiver TIA. A generic structure of an optical receiver is presented in the Fig.0.1.

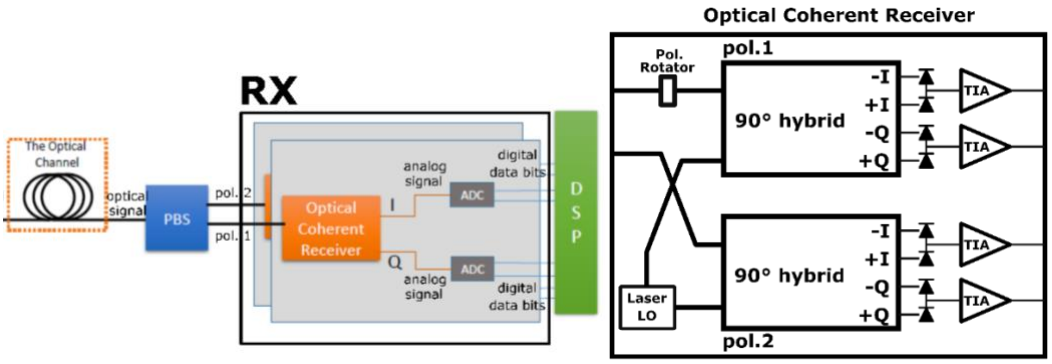

Fig.0.1 Basic scheme of an optical coherent receiver

After a demodulation of the optical signal realized by an 90° hybrid, the signal is converted in the electrical domain by a photodiode. Then its current is amplified and converted into voltage by the TIA. This device has to be characterized by a wide BW of the order of decades of gigahertz, a low noise in order to keep intact the safe the information carried by the signal, and a very high linearity to prevent the information carried by the coherent modulation. The presence of non-linarites and noise degrades the constellation and the BER as the Fig.0.2 shows.

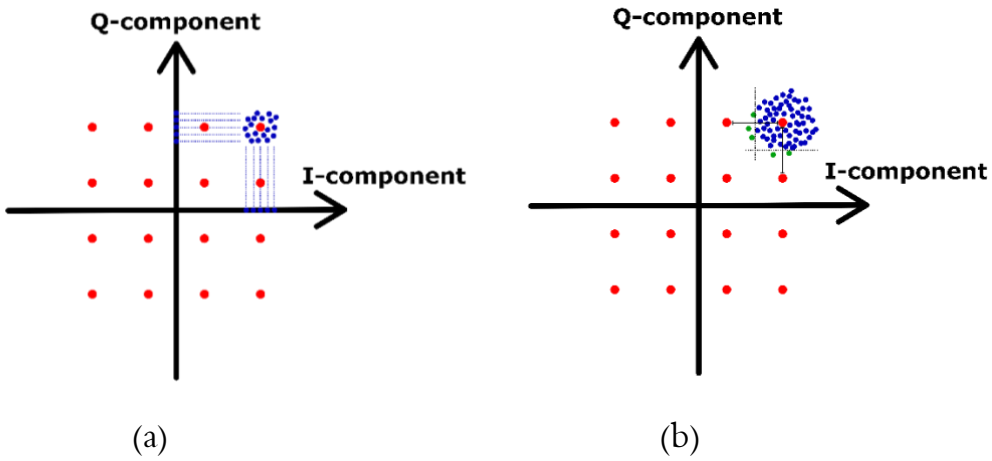

Fig.1.8 The non linearity effect on the constellation (a)
and an excessive non linearity that provide an incorrect decodification of the symbol (green dots) (b)

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Dan Li, Gabriele Minoia, Matteo Repossi, Daniele Baldi, Enrico Temporiti, Andrea Mazzanti, Francesco Svelto "A low-noise design technique for high-speed CMOS optical receivers" IEEE JOUTNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 6, JUNE 2014

RESEARCH ACTIVITY: The optoTIA

During this year I concluded the design, layout and optimization of a TIA whose structure is represented in the Fig.1.1.

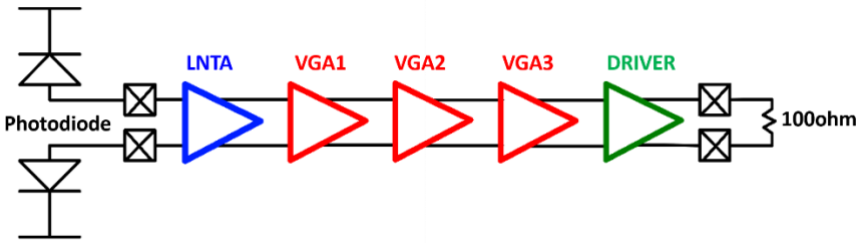

Fig.1.1 Block scheme of the designed TIA.

Five stages can be identified: the LNTA, three VGA and a DRIVER. after a deep analysis of the VGA's topologies, the selected one for this TIA is gilbert cell, reported in Fig.1.2. The DRIVER has to provide the matching with a 100 ohm differential at the output. This requirement is achieved by an active termination as the Fig.1.3 shows.

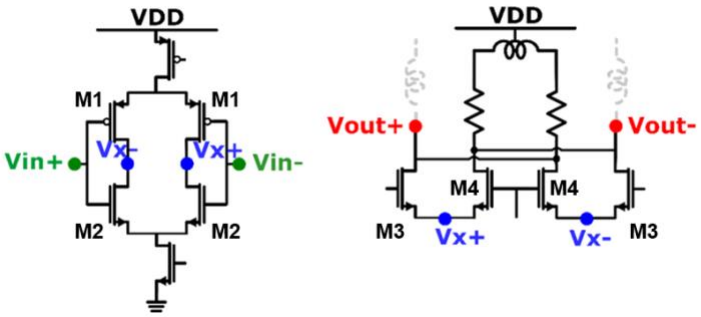

Fig.1.2 Schematic of the VGAs; it is realized by a first stage, and a second one that provide variability of the gain by a gilbert cell structure.

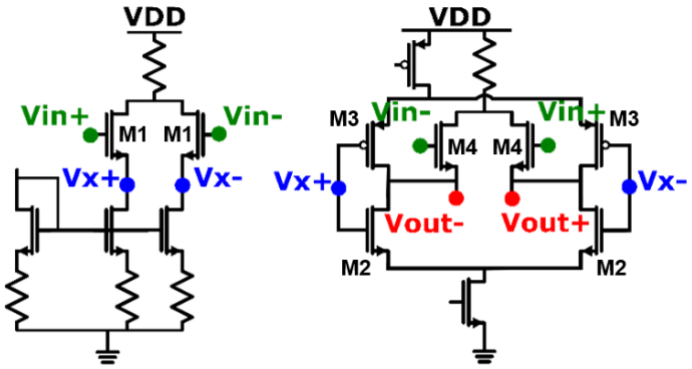

Fig.1.3 Schematic of the DRIVER with active termination realized by M3; its output impedance is mostly provided by $\frac{1}{gm_4}$.

The most innovative part of the design is focused on the LNTA. This topology is based on a Common Gate, where the current mirror is deleted thanks to the PN structure, reducing in this way its noise reported to the input. Usually the optical TIA are strongly BW limited due to the presence of the Photodiode that can be modeled by a big capacitance, that is added to the capacitances of pad and ESD. The positive feedback reduces the input resistance adding a negative conductance in parallel to the standard 1/gm. Looking to the Fig.1.4, we get that the input impedance becomes equal to $\frac{1}{g_{tot}} - g_2 * \frac{R_L}{g_{tot}}$, where $g_{tot} = g_1 + g_2$, $g_2 = g_{2_n} + g_{2_p}$ and $g_1 = g_{1_n} + g_{1_p}$.

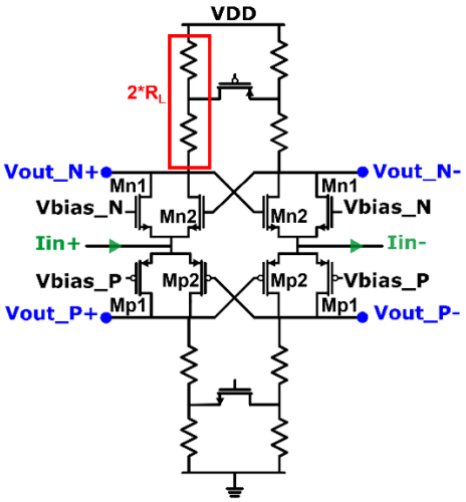

Fig.1.4 Schematic of the first stage of the LNTA;
its name is Common Gate Cross Drain (CGxD).

The stability of the loop is ensured when $g_2 * R_L < 1$, it means that if $g_2 * R_L = 0.5$ the input impedance is halfed. The trade off of this topology is linked to the noise and the output pole. To reduce the load of the next stage to the LNTA, the four outputs are combined by a PN source follower whose schematic is reported in Fig.1.5.

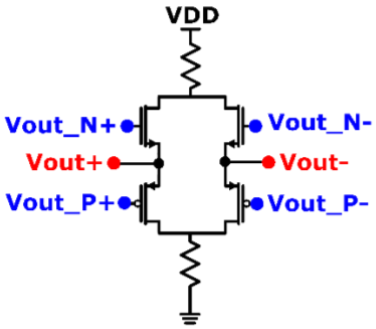

Fig.1.5 Schematic of the PN source follower, it is the second stage of the LNTA
and it combines the four outputs of the CGxD.

The post layout simulations of the TIA has a BW equal to 43GHz with a peaking of 3dB, average input referred noise equal to $\frac{17pA}{\sqrt{Hz}}$ at maximum gain and a maximum THD equal to 1.5% at 500mVpp differential output voltage. The transfer function and the S22 are plotted respectively to the Fig.1.6 and Fig.1.7

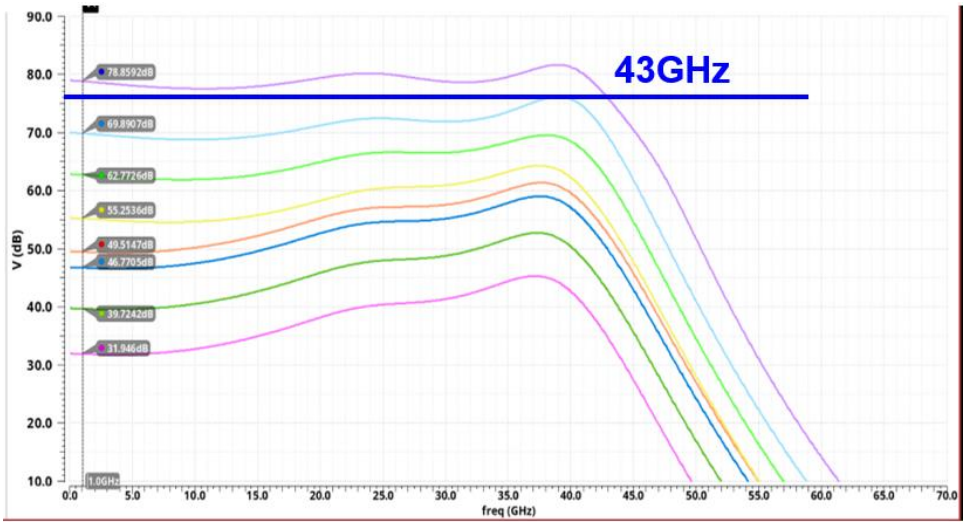

Fig.1.6 Transfer function of the TIA; it shows a BW of 43Ghz and a peaking at maximum gain equal to 3dB.

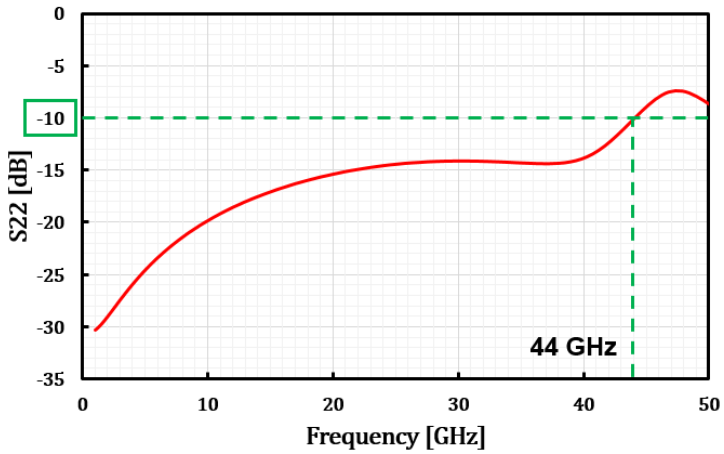

Fig.1.7 S22 in function of the frequency.

In the presented design the BW extension technique used is based on the triple resonance peaking by customized inductors in order to achieve a higher self-resonance frequency.

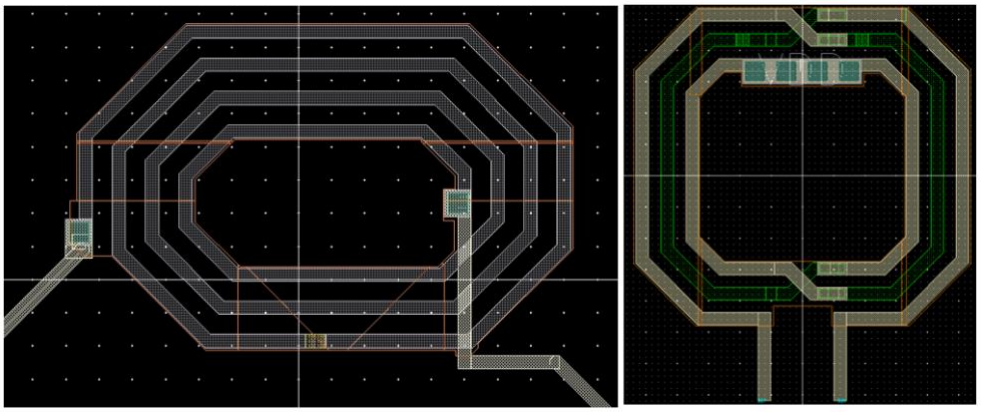

Fig. 1.8 Layout of the custom inductors. For the single ended inductor is used the AP metal (aluminum), while the differential inductors are realized by the metal 8 and metal 7 .

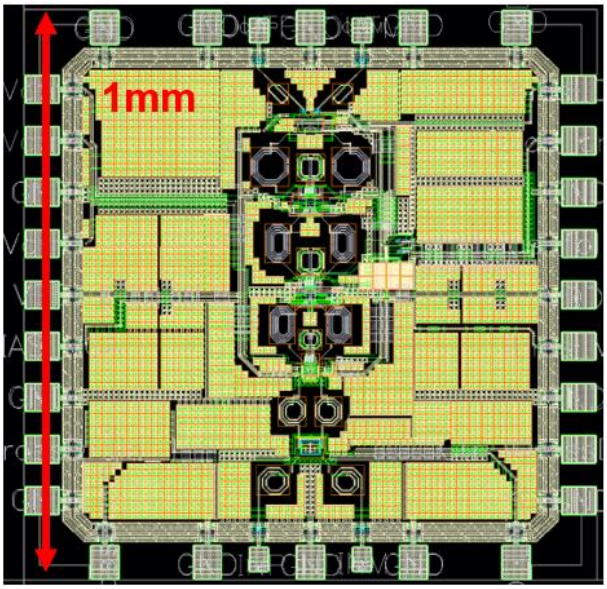

Fig.1.9 Top view of the chip.

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EDUCATIONAL ACTIVITIES

PhD SCHOOLS:

- SIE 2019 ROME, "*Electronics around the Earth*", University of Roma-TOR VERGATA, Rome, Italy;
- TOM Milan 2019 SESSION 1 MAY, "*Topics in microelectronics*", University of Milan-Bicocca, Milan, Italy;

SEMINARS:

- "*Extremely High Frequency Integrated circuits for emerging communication networks*", 16/01/2019, Pavia;
- "*Bosh Sensortech GmbH*", 19/12/2018, Pavia;
- "*Image sensors: challenges and applications*", 14/01/2019, Pavia;
- "*Introduction to DSP based serial Links*", 15/04/2019, Pavia;
- "*A 64Gb/s Low-Power Transceiver for short-Reach PAM-4 electrical Links 28 nm FDSOI CMOS*", 06/05/2019, Pavia;
- "*Wavelength switching technologies and coherent systems design in Photonic Backbones*", 06/06/2019, Pavia.

FRONTAL DIDACTIC SEMINARS:

- Tutoring for the courses of Electronic 1 and Algebra e Geometria.