UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

"High Frequency DC-DC Buck Converter Power Stage for Automotive Applications"

Tutor: Prof. Edoardo Bonizzoni

Ph.D. Student: Filippo Boera

Cycle: XXXIV (2018-19)

Research activity:

This research, done in collaboration with Infineon Technologies Italy, focuses on switching DC-DC buck converter for automotive applications in the post-regulated domain. The typical switching frequency of a DC-DC converter is a few MHz. By increasing the switcing frequency, a much smaller inductor can be used without degrading the ripple. Smaller inductors could be inserted inside the package, or even integrated, thus saving a lot of space and money. Efficiency is, of course, a key parameter, since a higher efficiency translates in less power wasted, so in less CO_2 consumption, which is a very critical specification for car manufacturers. The purpose of this reasearch is the study and the design of a Buck converter power stage switcing at 100 MHz with sufficient efficiency.

The proptietary Infineon technology for high voltage automotive applications features several mosfets models, each with different minimum dimensions, maximum V_{DS} sustainable, threshold voltage, capacitance etc. The models in the interest of this study are three: a "high voltage" (HV) mos with a maximum V_{DS} of 12 V and L_{min} equal to 1µm, a "medium voltage" (MV) mos with a max V_{DS} of 2.5 V and L_{min} equal to 400 nm, and a "low voltage" (LV) mos with a max V_{DS} of 1.5 V and L_{min} equal to 120 nm The first step of this study is to verify which topology works best as a power stage. Being this circuit intended to be in the post-regulated domain, the maximum input voltage should be between 2.7 to 5 V. To sustain 5 V there are two possible soluttions: either use the HV model or stack more MV and LV models. Different configurations lead to diferent results in terms of efficiency, both in the power switches and inverter chains. Four different schematics are shown in Fig. 1.

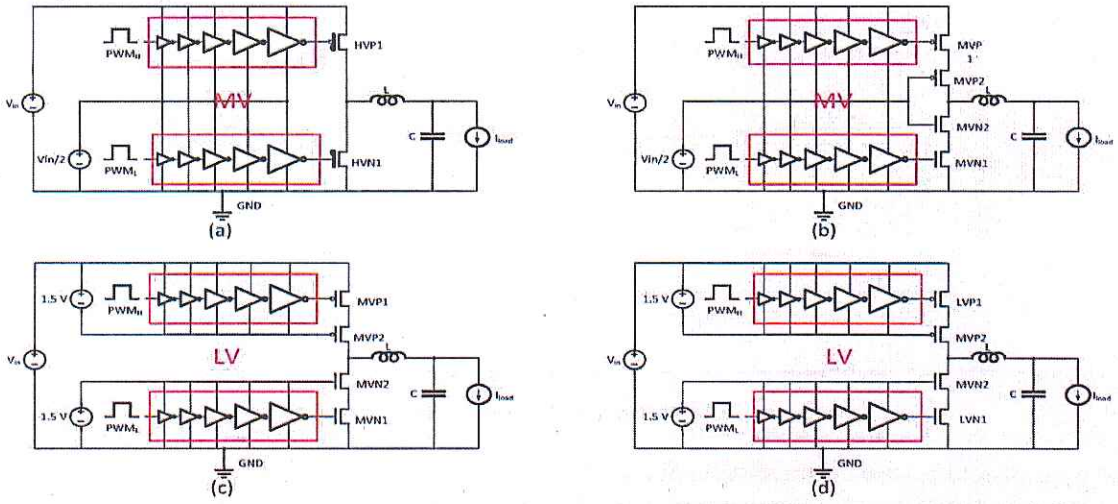

Fig. 1 – Four proposed schematics: (a) HV, (b) MV, (c) MW with LV driving, (d) Hybrid LV+MV.

The circuit in Fig. 1 (a) has the HV mosfets as power stage and the MV mos in the inverter chains. The HV mosfets can sustain any V_{in} in the desired range, but the length and the big gate capacitance of the HV mosfets cause an increase of both switching and conduction losses, resulting in a peak efficiency of only 73%. In Fig. 1 (b) the power stage has been realised by stacking two MV mosfets for each side, to ensure that the transistors can substain up to 5 V of V_{in}. This solution leads to an increase in the efficiency up to around 80%. Another slight improvement has been obtained by using LV mosfets for the inverter chain, as shown in Fig. 1 (c). In this way, the low supply of the high-side chain and the high side of the low-side chain cannot be both set as $V_{in}/2$, but have to be, respectively, $V_H = V_{in} - 1.5$ V and $V_L = 1.5$ V. With this adjustment, the efficiency rises to 82 %. Finally the schematic shown in Fig. 1 (d) is a hybrid solution for the power stage, cascading a LV and a MV mos. LV mosfets (smaller and with less parasitic capacitance) are used for switching, while MV are used for protection. Given the redued channel length of the LV mos, the eficiency rises, reaching the peak of 86%. The drawback of this solution is the limited sustainable input voltage, decreased from 5 to 4 volts. The simulated values of efficiency are shown in Fig. 2 as a function of the load current.

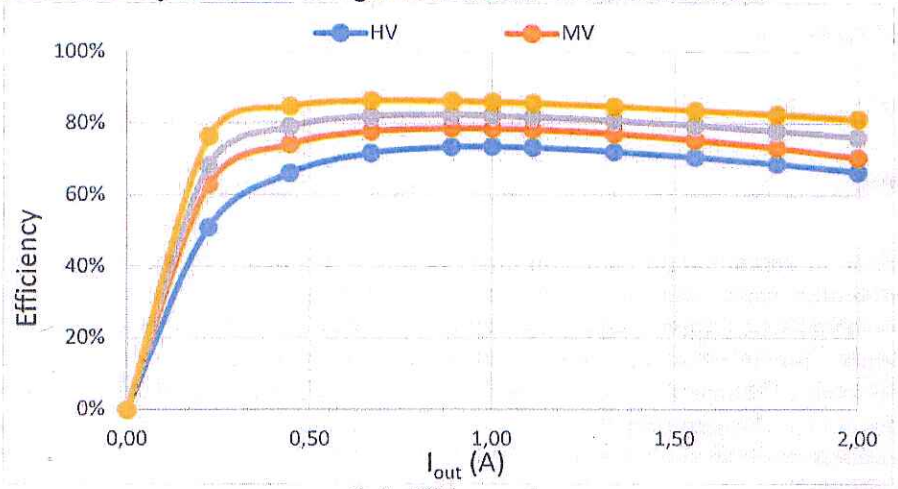

Fig.2 – Efficiency vs. I_{out}

Due to the significant increase of the efficiency, the Hybrid configuration is chosen for further development. The most critical issue to solve in this circuit is how to generate the two intermediate voltages V_H and V_L: if the voltage generators are not ideal, the high frequency, high load current, and big dimension of the power stage cause periodic jumps on the reference voltages around their nominal values when the circuit is switching. These jumps are due to the high current needed to charge/discharge the power transistors and the transistors in the pre-driver chains. Fig. 3 shows the effect on V_H and V_L when the ideal generators are substituted with real buffers.

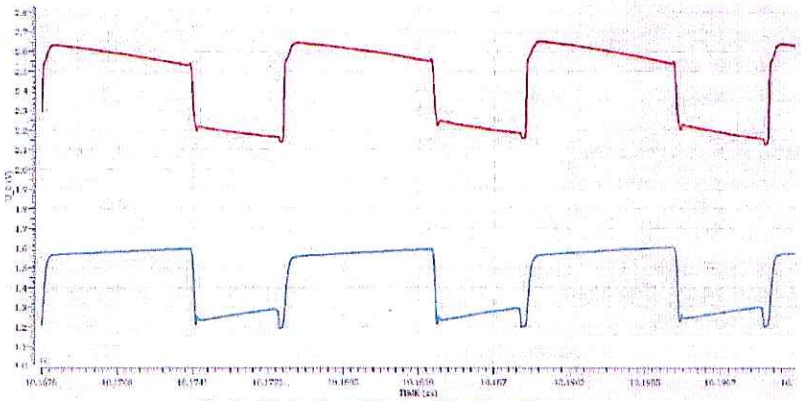

Fig.3 – V_H (red) and V_L (green) with real buffers.

These jumps could cause the breakdown of the transistors inside the inverter chain, or be the cause of a loss of efficiency, as the efficiency is maximized when the chains are driven with full swing. In this case, voltage

jumps are around 400 mV and the efficiency drops to 78%. It is clear that this issue must be solved (or at least mitigated) so that V_H and V_L stays as close as possible to V_{DD} – 1.5 V and 1.5 V respectively, but without exceeding the maximum value allowed by the technology. The scope of this research is to have as much integration as possible, so a fully integrated solution has been studied to compensate for this issue (without external caps). Notice that only V_H is considered, since it is the most critical between the two, due to the fact that it is variable while V_L is fixed at 1.5 V. Jumps on V_L are less critical, and do not compromise the functionality of the circuit or the safe operation of the transistors (LV transistors can actually sustain up to 1.65 V of V_{DS}). Also, as the two buffers are connected between them in the design, an improvement on V_H will impact also V_N, so adding a second control structure just for V_L could impact too much on the efficiency. The proposed idea is to generate a current pulse that will compensate for the jumps on V_H. To generate the desired pulse, the low clock signal (PWM_L in Fig.1) is given as an input of a NOR gate. The second input of the NOR gate is the same clock signal after passing through an inverter. The output of the NOR gate is an impulse every clock rising edge, with a duration depending on the delay of the inverter. This pulse is used to turn on an NMOS connected between V_H and ground that will sink current for a short amount of time (depending on the pulse width) every clock period, thus keeping the voltage V_H from going too high. This simple structure only allows to generate a pulse with fixed width. As an improvement, the width of the pulse is made adaptive, meaning that the delay of the mentioned inverter has to be variable. Fig. 4 shows the proposed control structure.

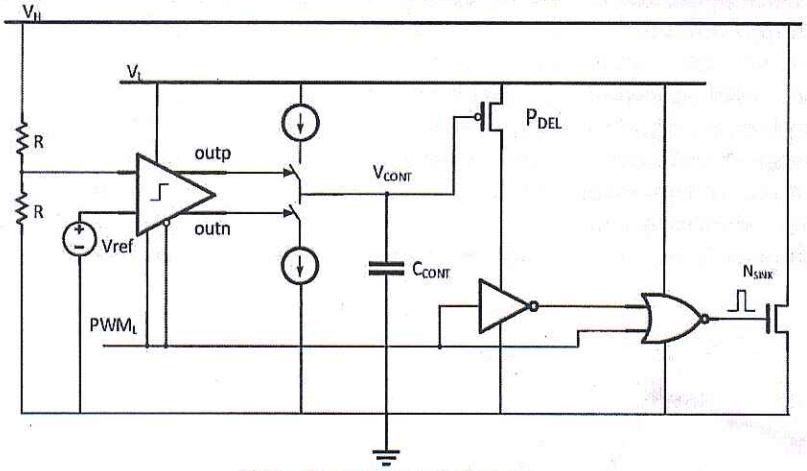

Fig.4 – Proposed control schematic

The voltage V_H is scaled and then compared with a reference through a clocked comparator. The output of the comparator are two signals "outp" and "outn". These two signals control to switches that will charge or discharge the capacitor C_{CONT}, thus setting the control voltage V_{CONT}. V_{CONT} sets the V_{GS} of the transistor P_{DEL}, so the current that P_{DEL} is sourcing to the inverter. Controlling the current of P_{DEL} results in controlling the delay of the inverter, and, consequentially, the duration of the pulse that turns on N_{SINK}: the longer the pulse, the longer the on-time of N_{SINK}, the more V_H will be lowered, and vice versa. The steady- state waveforms of V_H and V_L with the control technique is shown in Fig. 5.

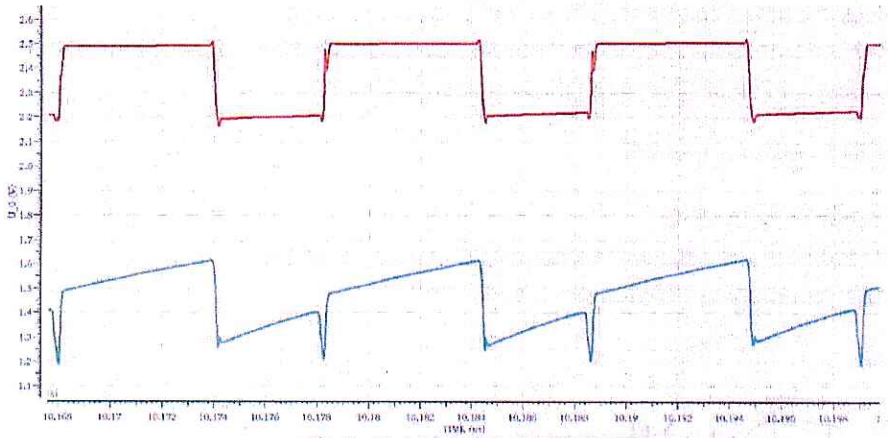

Fig. 5 – V_H (red) and V_L (green).

In the figure, the effect of the control can be seen on the rising edge. The current pulse keeps the voltage stable and lowers its average. The voltage swing on V_H is reduced of around 100 mV with respect to Fig. 4. At the same time the average of V_L is higher, improving the efficiency. The transistor N_{SINK} is properly sized to avoid a current spike that is too high, and could lower V_H too much. The simulated efficiency is 82%.

Secondary research activity:

The purpose of the secondary research activity is to modify an already existing 100 KHz oscillator to reduce its current consumption from 2.6 µA to a maximum of 1 µA. The core of the oscillator is a traditional comparator that compares a switched voltage reference and a voltage obtained from integrating a switching current with a trimmable capacitance. Some straightforward methods to reduce the current are used (i.e. reducing the dimensions of the biasing mirrors, removing buffers that were useless for this applications, resizing of input pair of the comparator etc.). The current is easily reduced to around 700 nA at room temperature. The issue is the drift in frequency with temperature: at -40° the circuit showed a drift of -5%, which is unacceptable for the application. The ideas to fix this issue are two. The first is straightforward: to remove the switched reference resistors and corresponding bias mirror branch, and take the reference directly from the output resistive partition of the bandgap of the circuit. This adjustment has a double advantage: to provide with a temperature-independent reference and to further reduce the current consumption of the oscillator. However, the main contribution to the temperature drift comes from the trimmable capacitance. The drift in temperature could be avoided by using poly-poly capacitors, but such capacitors require a dedicated mask, hence increasing the cost of the chip. The proposed solution is to split the capacitance in two, and place the two halves in antiparallel configuration. Doing so, the half that has been placed "upside down" behaves like a depletion MOS: at low temperature the channel is shorter and the frequency is higher. With these adjustments the oscillator shows a frequency drift over temperature less than 2%, and the current consumption at room temperature is 660 nA. Fig. 6 shows the frequency output and current consumption over temperature.

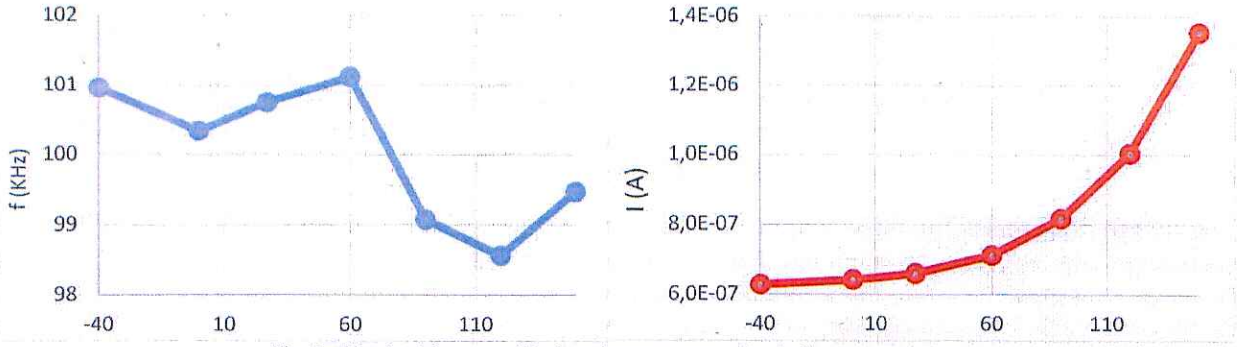

Fig. 6 – Simulated frequency (blue), and current consumtion (red) over temperature.

Future Work:

- Layout, tapeout and test of the DC-DC buck power stage.
- Design of control loop for next version of the Buck (power stage+control loop).
- Tapeout and test of the chip featuring the oscillator.

Accumulated Credits (6.5 CFU):

- Seminars (8): 1.6 CFU
- Ph.D Schools and Intensive Courses (19.5 hours): 3.9 CFU
- Ph.D Schools Final Exams (1): 1 CFU

Signature:

(Tutor)