UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

High Efficiency DC-DC converters for IOT applications

Tutor: Piero Malcovati

Dottorando: Thomas Eleftherios Dimitrios Kizas

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Dettagliare scopo dell'attività di ricerca dell'a.a. 2015/2016

The research activity during the academic year 2018/2019 was focused on the design of DC-DC converters for IOT applications for audio processing. The requested specifications are given in Table 1.

Table 1. Specifications for the DC-DC converter.

Battery Voltage (Nominal)	3.7 V
Battery Voltage (Range)	2.7-4.5 V
Outputs (#)	3
Outputs (load/Voltage/I_{outmax})	Digital /0.4-0.8V /100mA Bluetooth Module /1.2 V /50mA Other analog /1.8 V /50mA
Output voltage accuracy	±5%
Output voltage ripple	±10 mV
Inductor	Only 1, size 0402, size 0603 at worst
Capacitor	1 per output, size 0402
I_Q	<10μA
Noise restrictions: "Standby" (up to 1mA) "Running" (>3mW all rails)	None f_{sw} and spurious tones out of audible frequencies
Efficiency	90% at 10mA of load current
Wake-up time	<10ms
Technology	22nm-FDSOI

The input of the converter is expected to be a single cell Lithium-ion battery. The converter should be able to provide regulated power supply for load currents up to 50mA under 1.2 and 1.8V and up to 100mA for a supply rail which supports Dynamic Voltage Scaling for voltages between 0.4 and 0.8V. The quiescent current has to stay below 10μA to ensure long battery life. The efficiency target is ≥90% for a load current of 10mA. An important design constraint is related to the maximum physical size of the passives. A target size code of 0402 (imperial) has been chosen for both the inductor and the output capacitors with a backup for 0603 inductors due to the scarcity of inductors with L>100nH in 0402 packaging and the effects of this

constraint in the overall efficiency of the system. The power supply ripple has to be kept below 20mVpp. Last but not least, the switching frequency f_{SW} and its spurious tones have to be kept out of the audible frequency range to avoid interference (either conductive or through the generation of acoustic noise) on the 1.8 V rail which also supplies the circuits devoted to Audio Signal Processing when the system is not in standby mode.

According to the conducted literature research there is no published academic paper or datasheet of commercial product that can achieve such specifications with so small inductors. The low self-inductance values of 0402 inductors ($\leq$110nH) and their low saturation current impose a tight constraint on the maximum duration of a pulse, which in turn limits the amount of charge that the converter can move in a single cycle. As a result, the converter has to employ a higher switching frequency to meet the demands of the load. This makes the use of simple PWM in Continuous Conduction Mode unsuitable for light load operation due to the fact that gate driving losses do not scale with the output power and as a consequence they lead to a considerable reduction of efficiency.

The design of DC-DC converters is usually done with the help of hand calculations. However, the accuracy of such models (usually requiring the approximation of the system with a linear one) is limited to steady state operation. The lack of such tools has a considerable impact on the design process since there is no simple control scheme which can meet all the requested specifications and a combination of different control strategies in one system is required. For this reason, the first part of the research activity was focused on the creation of a library of high-level models of the building blocks used in the design of DC-DC converters.

These models are simple to use and parametrizable. They were written in VerilogA and can be simulated just like any other analog circuit with spectre. The cells model the ideal behavior of the respective blocks and also their most common non-idealities like the on/off resistance of switches, the offset and delay of comparators etc. The ability to easily extend these models to include the statistical parameters necessary for Monte Carlo simulations has also been demonstrated. Extra care was taken in the development of the models for the switches to ensure that they do not become a source of convergence difficulties. In total, 3 models were created. Two of them approximate the switch with a voltage-controlled resistor and use smootherstep and logistic sigmoid as smoothing functions. The third one models the behavior of an actual transistor and is based on the simple long channel transistor model of EKV.

The second part of the research was focused on the development of a DC-DC converter architecture suitable to fulfill the requirements.

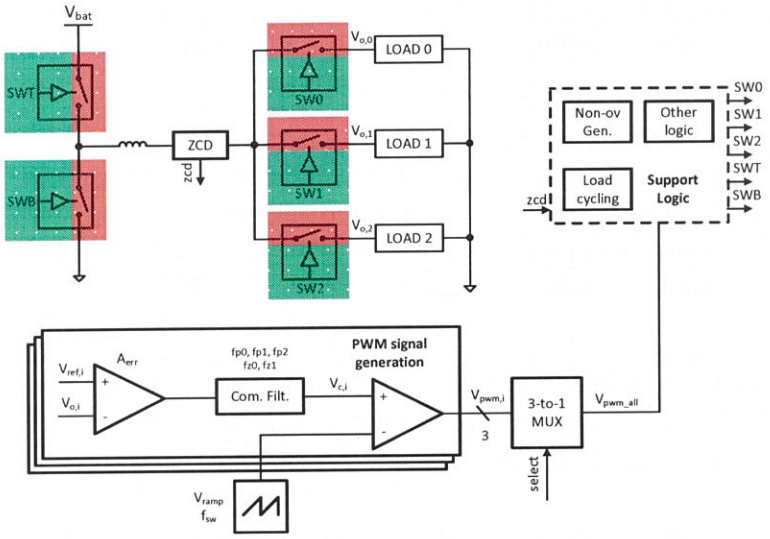

Figure 1. The block diagram of the architecture responsible for the "Running" mode of the converter.

A simplified block diagram of the proposed architecture (considering only "Running" operating conditions) is shown in Figure 1 and has the following features:

1. Inductor is timeshared between loads
2. DCM operation
3. One control loop per output
4. Constant frequency Voltage Mode PWM in "Running" mode
5. Switch Width Modulation
6. Comparator-based PFM in "Standby" mode

The choice for Discontinuous Conduction Mode operation is motivated by 3 factors. Firstly, the available 0402 inductors have very low self-inductance and low saturation current. This introduces an upper limit to the maximum charge transfer per cycle. Secondly, the gate capacitance of the transistors is quite high and as a result increasing the switching frequency to operate the converter in Continuous Conduction Mode would lead to unacceptably high gate-driving losses. Thirdly, DCM operation allows the designer to use independent control loops for every load.

The architecture employs two control strategies one for the "Running" and one for the "Standby" mode of operation. A constant frequency, Voltage Mode PWM strategy is used for the "Running" mode of the converter. The use of constant frequency PWM leads to a predictable noise spectrum and ensures that no significant noise is in the audible part. Voltage Mode control is used for its ability to work without requiring the implementation of noise-resistant, low I_Q current sensing blocks which would also be useless in "Standby" mode.

Constant frequency PWM has a limitation regarding the range of load currents that it can provide with high efficiency. This happens for two reasons. The first reason is that the power spent to drive the switches is always constant while the output power varies and this behavior leads to low light-load efficiency. The second reason is that the charging efficiency in inductive DC-DC converters reduces as the charging time of the inductor increases [Wens11]. As the output current increases, the duty cycle of the PWM increases and so does the ratio of conduction losses to charge moved per cycle. As consequence the high-load efficiency of the converter falls. The Switch Width Modulation technique [Amin18] can tackle this problem and increase

the range of load currents that the converter can provide with high efficiency without having to change the switching frequency. With this technique the switch is split in multiple parallel blocks and the converter chooses how many it needs to cycle to keep the conduction losses under control.

Constant frequency VM PWM is not suitable for operation in "Standby" mode for two reasons. First of all, maintaining constant switching frequency means that we will suffer from low light load efficiency unless we use Switch Width Modulation. Secondly, its is possible to implement a control strategy which uses Pulse Frequency Modulation with fewer and less power hungry building blocks. As a result the "always on" part of the control loop is smaller and consumes less power, a feature that is desirable for low I_Q designs like this. Therefore, the control for the "Standby" mode is realized through a simple PFM control mechanism which triggers a fixed-width current pulse if the comparator shows that the voltage of a rail is below the required value. The width of the pulse will be decided based on the requirements for ripple, the maximum standby current and the effect of non-idealities on the size of the transferred charge packet. The behavior of a mechanism like the above with a discrete-time comparator is shown in Figure 2.

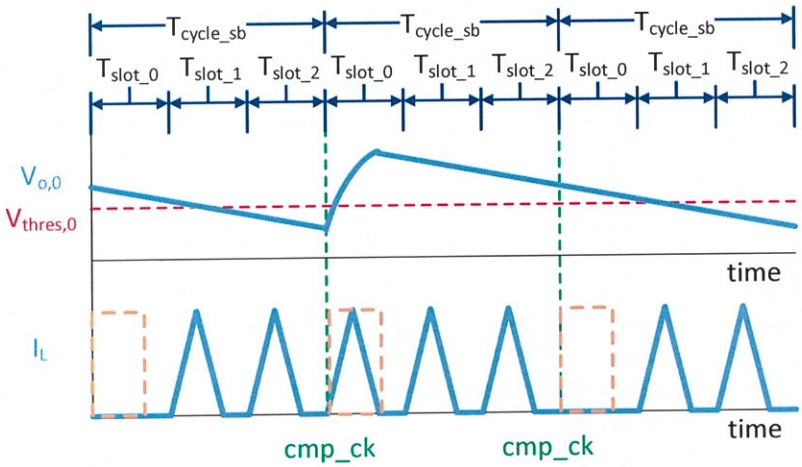

Figure 2. Operation of "Standby" mode PFM control strategy with a discrete-time comparator. I_L is the inductor current. A current pulse is sent to the respective load only when the comparator detects that $V_{o,0} < V_{thres,0}$.

CFU 2018/2019

- Scuole dott. Di Enti ricerca – Corsi intensivi CFR 9.4
- Seminari di Dottorato CFR 3.8

References

[Amin18]. S. S. Amin and P. P. Mercier, "MISIMO: A multi-input single-inductor multi-output energy harvester employing event-driven MPPT control to achieve 89% peak efficiency and a 60,000x dynamic range in 28nm FDSOI," *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 144-146.

[Wens11]. Wens M., Steyaert M. (2011) "Basic DC-DC Converter Theory". In: "Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS". *Analog Circuits and Signal Processing*. Springer, Dordrecht