UNIVERSITÀ DI PAVIA
Department of Electrical, Computer and Biomedical Engineering

Ph.D. activities report – 1st year

Matteo Pezzoli
Università degli Studi di Pavia
Microelettronica
XXXIV ciclo

AA 2018–2019

Arcadia

Introduction

The purpose of the Arcadia project is to develop a scalable, low power, fully depleted CMOS sensor compatible with standard CMOS fabrication processes. The project is founded by INFN and is pushed forward by a collaboration of various institutions and INFN research groups. My contribution on the project is the development and testing of various IP blocks that will be used in Arcadia and, eventually, will be part of the INFN portfolio on the used technology. As of today, the blocks I will develop and test are a bandgap voltage reference and a custom data line driver and receiver. At the end of the first academic year, the work done on this project has been the schematic of the bandgap reference and the schematic and layout of both the driver and receiver. The driver and receiver blocks will be integrated in an engineering run due to start around October 2019; all results presented in this report related to Arcadia are simulations only.

Bandgap reference

The implemented architecture is a current-mode bandgap reference that uses CMOS devices in sub-threshold region as active devices, as shown in fig. 0.1. The current-mode architecture permits

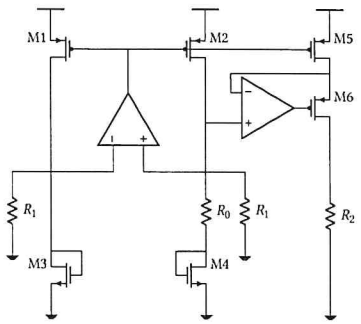


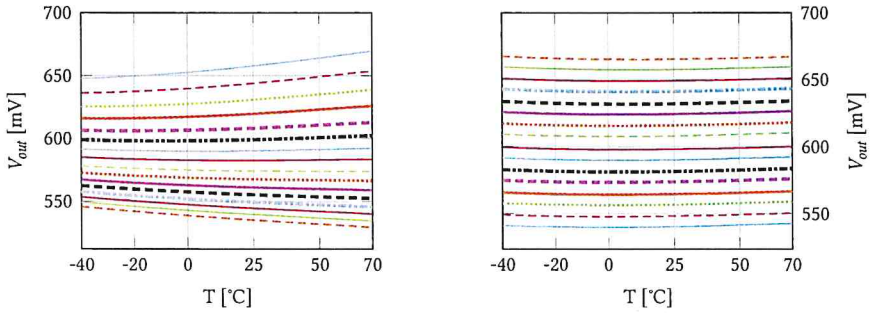
Figure 0.1 – Architecture chosen for Arcadia's BGR block

a good degree on control on the output voltage value, and usage of MOS instead of BJTs as active devices will cause the system to be more resistant to radiation induced damage, in particular to displacement damage[I]. The results obtained with this architecture are, in the best-case scenario of a typical corner simulation, a mean output value of 598.4 mV and a temperature coefficient of 25.4 ppm/°C. In order to add a degree of post-process tuning, two programmable resistor have been added to the schematic, respectively R_0 and R_2 in the schematic shown in fig. 0.1; the values of both resistors are set using 4 configuration bits each. R_0 is used to control the slope of the V_{out}/T curve, whereas R_2 is used to change the mean value of the V_{out}/T curve. Figure 0.2a and fig. 0.2b show the results obtained for different values of R_0 and R_2, respectively. As is to be expected, changing R_0 changes the slope of the V_{out}/T curve, but also changes the current flowing into R_2, meaning that R_0 causes a change in both the slope and mean of the output curve; this behavior, even though undesirable, can be easily fixed by counteracting the output mean change by acting on R_2 configuration bits.

Driver

The implemented driver functionality is built on a current-steering based on an H-bridge architecture, as shown in fig. 0.3a. The circuit also features a Common Mode FeedBack (CMFB) amplifier used to set the output common-mode to 450 mV, which operates by sensing the output common-mode

[I]Displacement damage refers to damage to the silicon lattice, mainly characteristic of high energy neutron irradiation, but in some cases can also be caused by charged particles incidence.

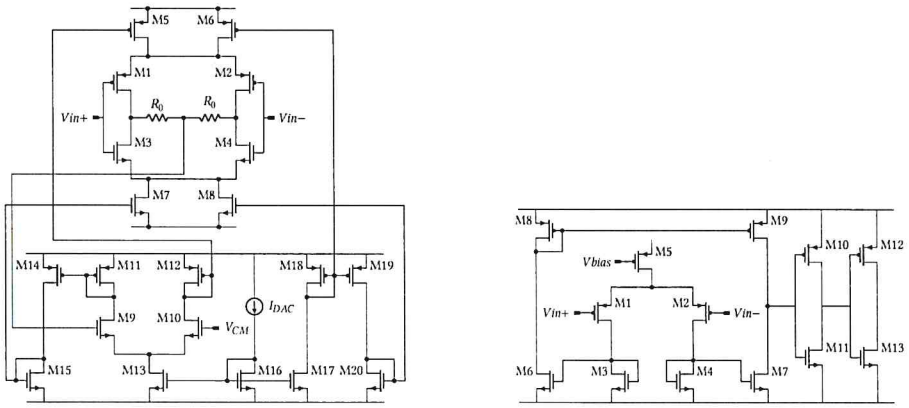


(a) Simulation results changing the slope controlling programmable resistor.

(b) Simulation results changing the mean controlling programmable resistor.

Figure 0.2 – Bandgap voltage reference simulation results.

through a resistive divider and comparing it to a common mode reference; the CMFB amplifier current is then mirrored into the driver structure by means of M5 and M7 current mirrors. The



(a) Schematic of implemented differential line driver.

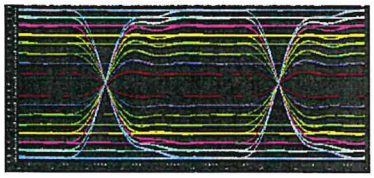
(b) Schematic of implemented differential line receiver.

Figure 0.3 – Transmitter and receiver schematics.

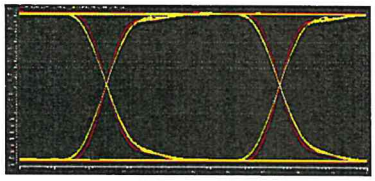
driver was designed for 2 Gbit/s operation, with a current of 2 mA, but a low-power mode has been requested by the collaboration. Hence, the current implementation of the driver features a DAC-controlled reference current, which is in turn used to generate all biasing current in the circuit. Said DAC is a 3 bit current switching architecture; the effects of the DAC operation are mainly observable in the driver current, which can be changed from a maximum value of 2 mA to a minimum of 250 µA. Simulated eye diagrams using a 2 Gbit/s PRBS as input, for all DAC words, are shown in fig. 0.4a, while fig. 0.4b shows a comparison, for the highest current setting, between the schematic simulation and the post-layout one. A layout for this architecture has been realized in collaboration with INFN Torino, covering an area of 55 $\mu m^2 \times 36\ \mu m^2$.

Receiver

The receiver has been developed as a single-ended amplifier feeding an inverter chain , as shown in the schematic presented in fig. 0.3b. Results of simulations using the already described transmitter are shown in the eye diagrams of fig. 0.5a. Simulations have been performed using the described driver as input for the receiver. A comparison between schematic and post-layout simulations are presented in fig. 0.5b. The results in fig. 0.5a show the eye diagrams down to a driver current of 750 µA; below said driver current, eye parameters start to degrade, unless the transmission frequency



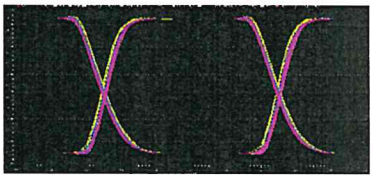
(a) Driver simulation results for different current configuration bits.



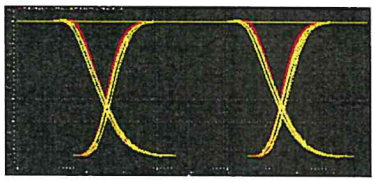
(b) Comparison between simulated TX output of schematic (red) and PLS (yellow).

Figure 0.4 – Custom differential line driver simulation results.

is lowered down to 1 Gbit/s. In order to add this circuit to a first engineering run, this first version has been submitted as is; the reason behind this choice has to do with the fact that a mode that requires a low current consumption will likely be coupled with a lower frequency in the digital blocks. In any case, this problem will be worked upon in the next version of the receiver. A layout



(a) Receiver simulation results for different driver current configuration bits.



(b) Comparison between simulated TX output of schematic (red) and PLS (yellow).

Figure 0.5 – Custom differential line receiver simulation results.

has been completed for this block as well, covering an area of $20\,\mu m^2 \times 12\,\mu m^2$.

PFM3 testing and characterization

Introduction

As a part of the PixFEL project, PFM3 is a 32x32 pixel matrix implementing a dynamic compression of the input signal based on the non-linear characteristic of a MOS capacitor. The non-linear capacitor is used as a feedback device in a charge sensitive amplifier in order to allow coverage of the wide input range, expected to be from 1 to 10^4 photons. The chip analog chain consists of the aforementioned CSA, a time-variant filter and a 9-bit SAR ADC; the characterization work performed so far has been focused on the amplifier block only, whose schematic is shown in fig. 0.6.

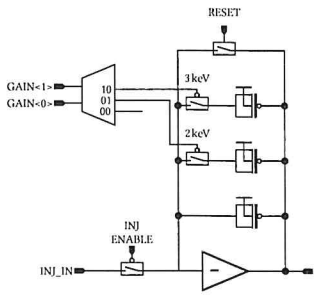
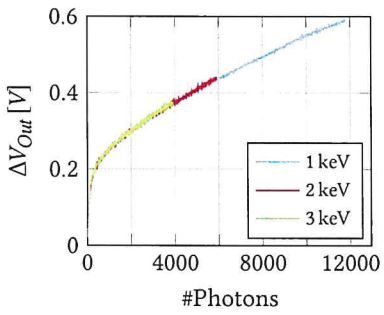


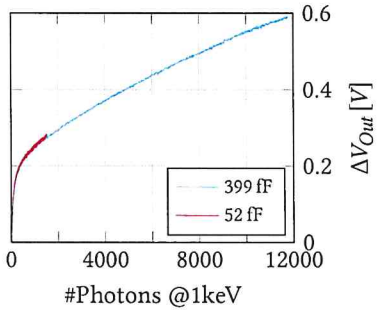
Figure 0.6 – Simplified schematic of the gain settings for PFM3 charge amplifier.

Measurements

The measurements shown in this section have been performed with the goal of characterizing and comparing the different gain settings and injection capacitances present on PFM3's CSA block. Figure 0.7a shows the output measurements for a sweep on the input signal going from 0 V to 1.3 V (equivalent photon count is dependent on the chosen gain setting); gain settings behave as expected across the 2 channels tested on both available PFM3 chips. Figure 0.7b shows a comparison at a fixed gain setting, for different injection capacitances; here the measurements seem to be coherent when all pixels are active, but measurements comparing different injection capacitances begin to differ when the matrix is partially disabled. In order to gauge the impact that the temperature has on the



(a) comparison of CSA outputs using the 399 fF injection capacitance, using 1 keV, 2 keV and 3 keV gain settings.



(b) Comparison between different injection capacitances, using 1 keV gain setting.

Figure 0.7 – PFM3 characterization results.

output characteristics, a set of measurements has been carried out in the INFN Pavia thermostatic chamber. A subset of these measurements has been reported in fig. 0.8; the output characteristic seems to have undergone expected changes, such as a shift in the curve kink, but the behavior still differs from previous measurements and simulations; the reason is still being investigated.

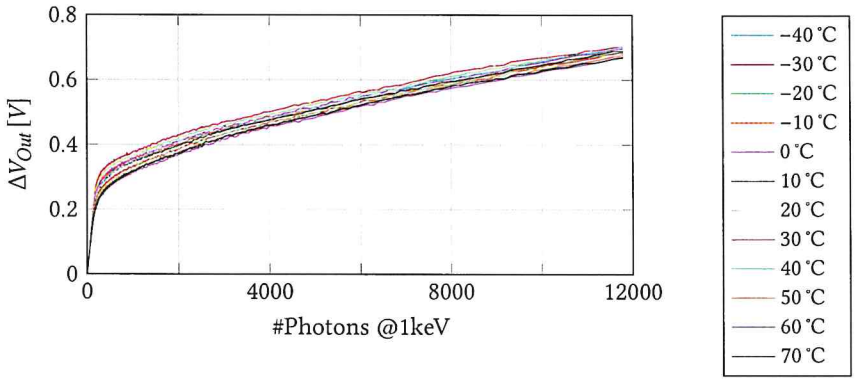


Figure 0.8 – Comparison between different thermostatic chamber temperatures, for a fixed injection capacitance and gain setting.

Pavia, 17th September 2019

Tutor signature

Tutor signature