UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

"BiCMOS Integrated Circuists for 5G applications"

Tutor: Prof. Andrea Mazzanti

Ph.D. Student: Domenico Riccardi

Cicle: XXXIV **Year**: I (2018-19**)**

Research activity:

- VCO Array

The ever-growing mobile data traffic is demanding a continuous innovation in wireless communication, and the next-generation 5G mobile networks are expected to provide ultra-high data rates. However, the use of spectrally efficient high-order modulations like 64 QAM sets challenging phase-noise specifications for integrated frequency synthesizers.

As an example, the estimated required phase noise at 1 MHz offset from a 20 GHz carrier for negligible EVM degradation with BER=10^{-6} is around -102 dBc/Hz for QPSK and -114 dBc/Hz for 64 QAM (assuming a phase noise integration bandwidth from 250 kHz to 250 MHz).

Phase noise $L(\Delta f)$ in an LC oscillator can be described with good approximation by Leeson's equation:

$$L(\Delta f) = 10\log\left[(1+F)\frac{4kTR_T}{A_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2\right] \qquad (1)$$

where Δf is the frequency offset from the carrier f_0, k is the Boltzmann's constant, T the absolute temperature, Q the tank quality factor, A_0 is the amplitude of oscillation, R_T the tank parallel resistance, and F is the oscillator excess noise factor.

It is clear from Eq. (1) that phase noise decreases by 20 dB/dec increasing the amplitude of oscillation A_0, and this is exploited in GaAs transistors, which can sustain higher supply voltages compared to silicon, achieving up to 10 dB better noise results.

If we focus on silicon technologies, though, for maximum output voltage swing, the minimum achievable phase noise is determined by the minimum realizable inductor, still displaying the highest Q value offered in the process. Indeed, assuming $R_T = 2\pi f_0 QL$, Eq. (1) shows the dependency on L/Q which must be minimized. However, when reducing inductance, Q tends to decrease because of both the magnetic coupling between the two halves of the inductor and interconnection parasitic resistance.

To overcome this limit, a multi-core approach may be exploited, leading to a reduction of the tank impedance R_T at costant Q and costant oscillation swing A_0. Increasing the number of cores by N, R_T is scaled down by N and so is the phase noise, since replacing $A_0 = R_T I_{\omega_0}$ Eq. (1) can be rewritten as:

$$L(\Delta f) = 10 \log \left[(1+F) \frac{4kT}{R_T {I_{\omega_0}}^2} \left(\frac{f_0}{2Q\Delta f} \right)^2 \right] \qquad (2)$$

where I_{ω_0} is the fundamental harmonic component of the tank current.

Moreover, the switch-coupled multi-core LC VCO, proposed in this work, allows to achieve ultra-low phase noise and scalable noise performance in a power efficient way. Indeed, doubling the number of active cores the phase noise is halved, but the power consumption is doubled, thus keeping the FoM constant. A programmable number of active cores (16, 8, 4, 2, 1) allows to accommodate the system requirements adaptively, performing always the needed phase noise and saving power.

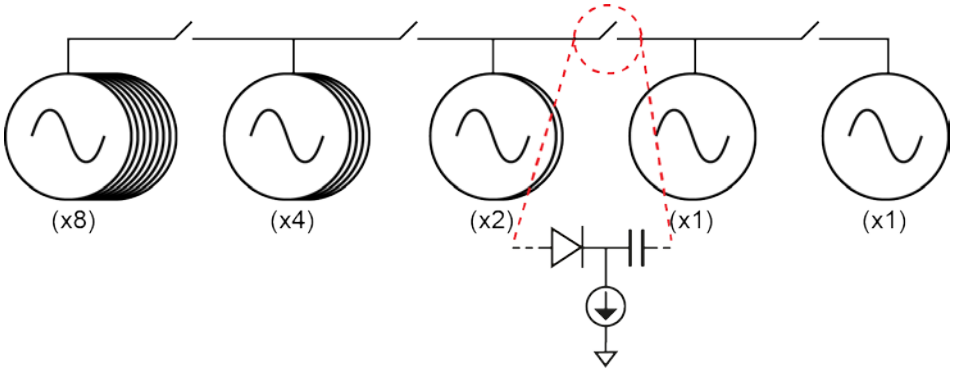

Figure 1. Switch coupled 16-cores VCO block diagram. Switch schematic in the insight.

In this work, an innovative switch design has been used, involving diodes instead of transistors (Figure 1), with many benefits. Indeed, mismatches among oscillator tanks lead to a phase-noise penalty that depends on the coupling resistance and can be minimized selecting a low ON resistance of the switches. Diodes can easily offer a low ON resistance, avoiding the use of large transistor switches with large parasitic capacitances that lead to tuning-range reduction. Furthermore, diodes can sustain high voltage swing, thus allowing to use the 2.5 V voltage supply of the 55nm BiCMOS technology.

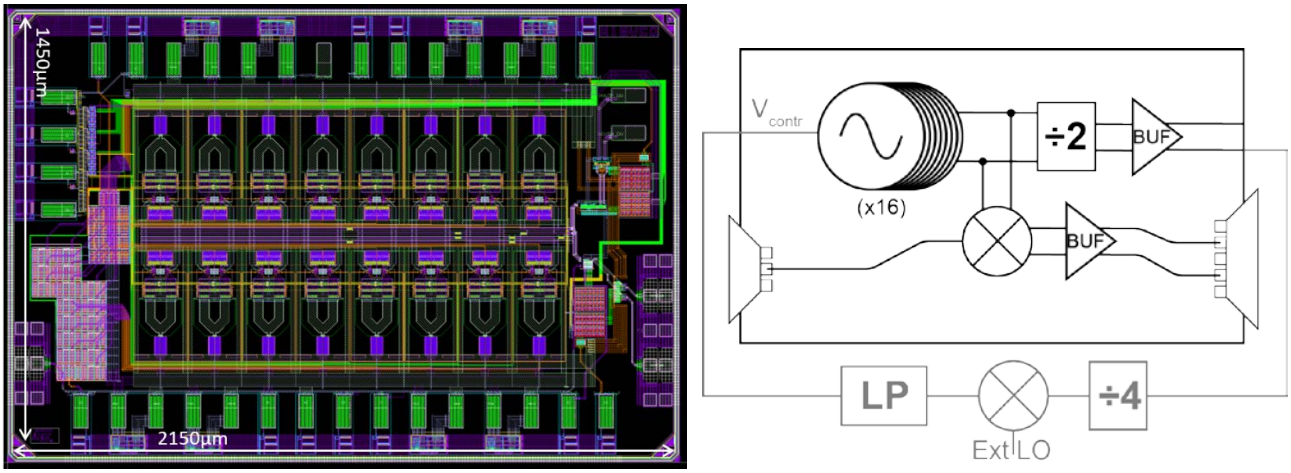

Figure 2. [Left] Layout of the chip and [right] block diagram (in grey the external components).

Figure 2 shows the layout of the chip which, as illustrated in the block diagram, incudes besides 16 active cores, a frequency divider by two and a mixer for down-conversion, to provide two separated output paths for measurement purposes. To keep the output frequency fixed, a PLL is planned to be built exploiting an external frequency divider by four and an external mixer as phase detector.

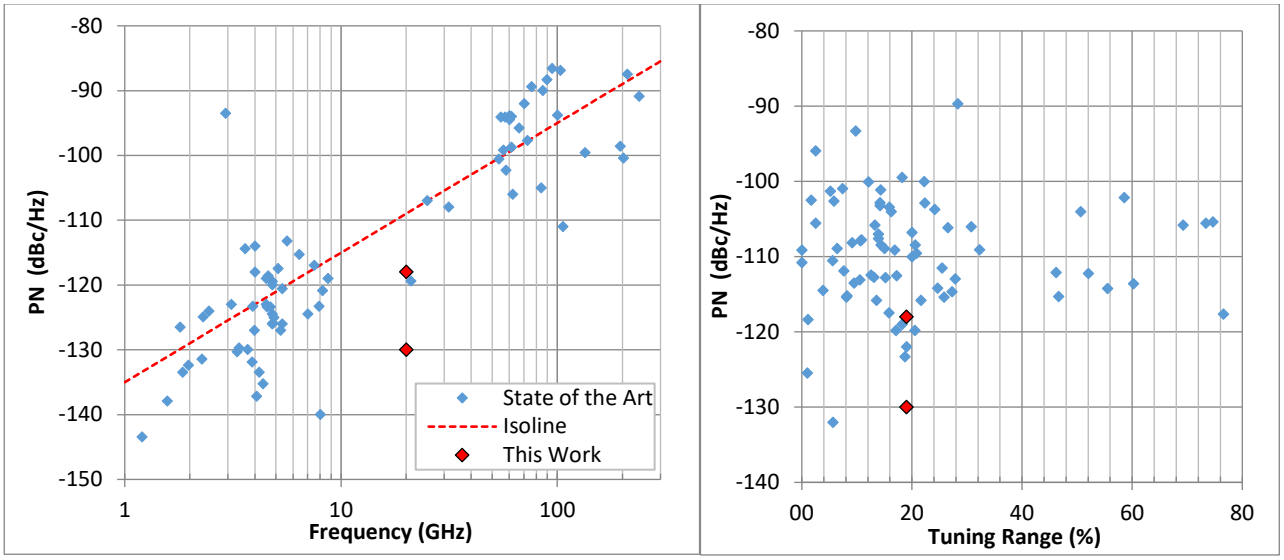

Figure 3. [Left] State of the Art LC-oscillator Phase Noise at 1 MHz offset versus carrier frequency. [Right] State of the art Phase Noise normalized to a 20 GHz carrier versus carrier frequency tuning range.

Post layout simulations show a phase noise value at 1 MHz offset from a 20 GHz carrier ranging from -118 dBc/Hz (1 core ON) down to -130 dBc/Hz (16 cores ON), which is among the best results considering the state of the art (Figure 3), the best ever if tuning range is taken into account (19% tuning range in this work).

Both the tuning range and the FoM of -185 dBc/Hz remain constant turning on and off the cores.

- BALUN

Baluns are used to provide conversion between an unbalanced input signal and balanced output signals. This is a key functionality in many circuits such as differential amplifiers and balanced mixers.

Generally speaking, passive baluns can be divided into lumped element and distributed baluns. In this work an analysis of both topologies has been performed, comparing the advantages of a lumped element structure such as compact size and possibility to match complex loads, and the advantages of distributed baluns, e.g. broader bandwidth and better balun performances.

A conventional Marchand balun has finally been included in the design of a D-band differential power amplifier. This circuit, whose layout and block diagram are depicted in Figure 4, provides balanced signals at the two output ports (P2 and P3) when driven from an unbalanced signal at the input port (P1). It consists of two sets of quarter-wavelength coupled lines connected together.

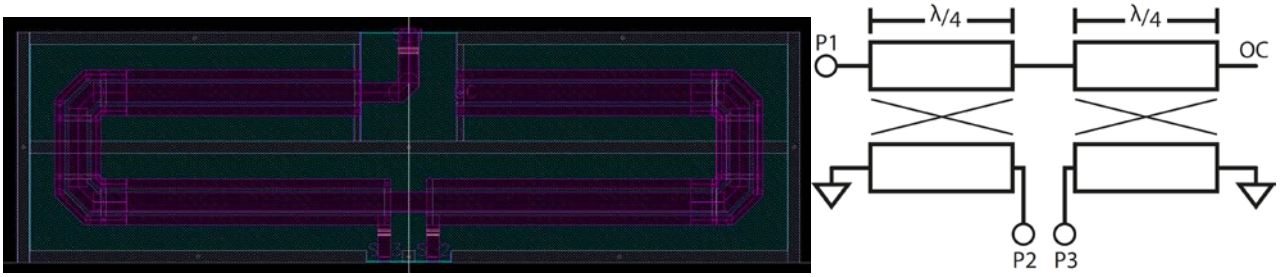

Figure 4. [Left] Layout of the chip and [right] block diagram.

In the table below are reported all the performances of the balun, according to a 3-port S-parameter simulation.

$\|S_{11}\|$	$\|S_{d21}\|$	$\|S_{d2d2}\|$	$\|S_{21}\|-\|S_{31}\|$	$\angle S_{21}-\angle S_{31}$
-40dB	-1.09dB	-39dB	0.05dB	180°

Where S_{d21} is the insertion loss, calculated as a mixed S-parameter (when port P2 and P3 are driven differentially) through the formula: $S_{d21}=(S_{21} - S_{31})/\sqrt{2}$. While S_{d2d2} is the differential-mode S-parameter: $S_{d2d2}=(S_{22} + S_{33} - S_{32} - S_{23})/2$

Accumulated Credits (7,3 CFU):

- Seminars (12): 2,4 CFU
- Ph.D Schools and Intensive Courses (19,5 hours): 3,9 CFU
- Ph.D Schools Final Exams (1): 1 CFU

(Student) (Tutor)