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1st Year Phd Report

A wideband open-loop baseband filter for 5G wireless applications

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INTRODUCTION

Fifth-generation mobile communication systems need to provide higher data-rates. The easiest way to achieve it is to use larger channel bandwidths, following the same trend of previous generations. Even if not yet standardised, 5G can include lower frequencies (FR1), below 6 GHz, and higher frequencies (FR2), above 24 GHz, with channel bandwidths in the order of GHz at mm-wave and narrower channels ($\backsim$100-200 MHz) below 6 GHz. So, in the case of higher frequencies, a baseband filter with bandwidth in the order of GHz is desirable. Even though, conventional TIAs based on shunt feedback topologies can have good linearity and low noise, for filter bandwidths exceeding 100 MHz the required OTA gain-bandwidth product (GBW) exceeds several GHz, resulting in very large current consumption. Moreover, with increased RF frequency, the impedance Z_D goes down (see Figure 1), consequently lowering the loop gain of the TIA which results in the OP-AMP noise amplification. So, with the increase of the channel bandwidths it becomes very challenging to fullfil the requirements of the TIA. A solution adopted is to use an open

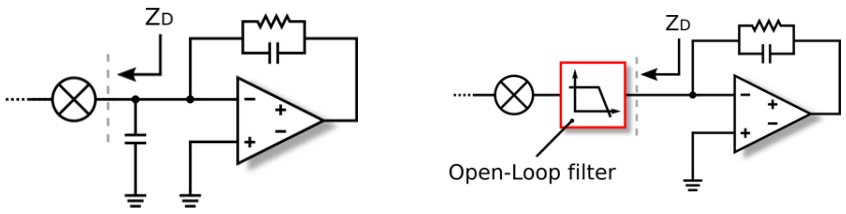

Figure 1: introduction of open loop filter in front of baseband TIA.

loop filtering TIA in front of the closed loop TIA that provides a 2^{nd} order filtering of interferers and offers a high output impedance. As a result, the requirements of the closed loop TIA following the open loop filter becomes highly relaxed, since it has to provide one pole instead of 3.

OPEN LOOP BIQUAD

An open loop biquad promising for large bandwidth is implemented with a common-gate (CG) stage (see Figure 2a). An explicit gate-source capacitance,

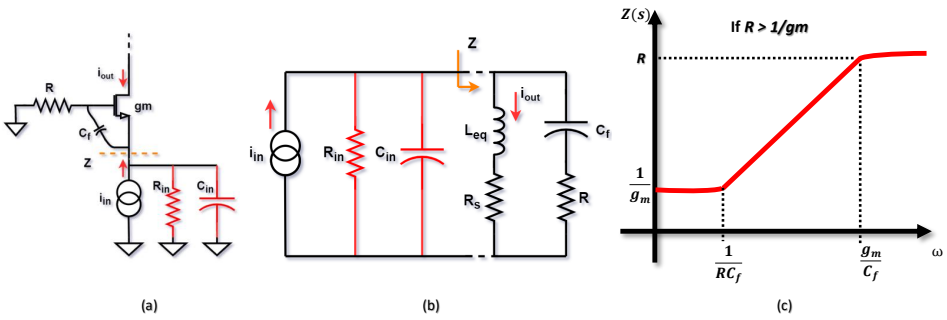

Figure 2: a) Common Gate stage with feedforward capacitor C_f. b) equivalent model. c) impedance at source of CG stage.

C_f, is placed on the CG, shunting the transistor V_{gs} at high frequency. If it is made sure that $R > 1/g_m$, it produces an inductive behaviour in its input impedance $Z(s)$, where

$$Z(s) = \frac{1 + sC_fR}{g_m(1 + \frac{sC_f}{g_m})}, \tag{1}$$

The equivalent inductance is given by the slope of Z(s), $L_{eq} = \frac{RC_f}{g_m}$ with its losses, represented by R_s in the equivalent model, whose value is given by $\frac{1}{g_m}$. Adding a shunt capacitance, C_{in}, towards ground, the CG current is 2^{nd} odered low pass filtered. The transfer function, i_{out}/i_{in} is

$$\frac{i_{out}}{i_{in}}(s) = \frac{g_mR_{in}}{1 + g_mR_{in}} \frac{1}{1 + s(\frac{RC_f + R_{in}C_f + R_{in}C_{in}}{1 + g_mR_{in}}) + s^2(\frac{RC_fR_{in}C_{in}}{1 + g_mR_{in}})} \tag{2}$$

where

$$\begin{aligned} \omega_o &= \sqrt{\frac{(1 + g_mR_{in})}{RC_fR_{in}C_{in}}}, \\ Q &= \frac{\sqrt{(1 + g_mR_{in})(RC_fR_{in}C_{in})}}{RC_f + R_{in}C_f + R_{in}C_{in}}. \end{aligned} \tag{3}$$

This solution can reach very wide bands but suffers from two main drawbacks: 1) a low in-band input impedance requires a large currrent in the CG branch, with considerable noise from the load resistance; 2) the low driving impedance limits the achievable Q of the biquad poles and consequently the selectivity.

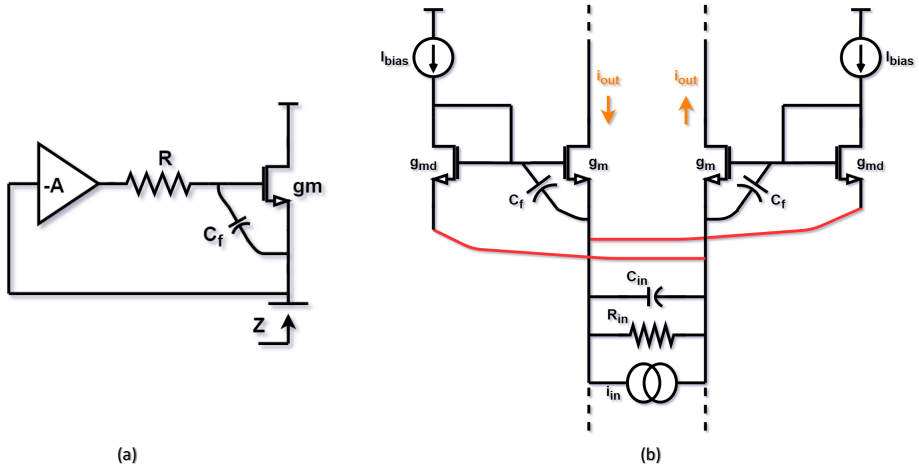

Figure 3: a) regulated cascode architecture. b) implementation of gain stage A with cross-coupled diode-connected transistor.

So to solve the first issue, a regulated cascode architecture that boosts the CG V_{gs} by (1+A), as shown in Figure 3a, is used. Here the in-band impedance of the CG $(1/g_m)$ is lowered by a factor (1+A), allowing to lower the CG current and the noise of the load resistance by the same factor. Inductive behaviour is again achieved through feed-forward capacitor C_f. An amplifier, A, is realised through a cross-coupled diode connected transistor (see Figure 3b) and its gain is equal to 1. As a result, the noise of the load resistor goes down by a factor of 2.
In order to solve the second issue, a negative capacitance is added at the input of the filter. Negative capacitance is realized through the use of Miller effect with positive feedback. As illustrated in Figure 4, two capacitors are placed between the inputs and their corresponding non-inverting outputs. The impedance, Z_{in}, seen at the input is given as

$$Z_{in} = \frac{1}{s(1 - g_m R)C} + \frac{R}{(1 - g_m R)}. \tag{4}$$

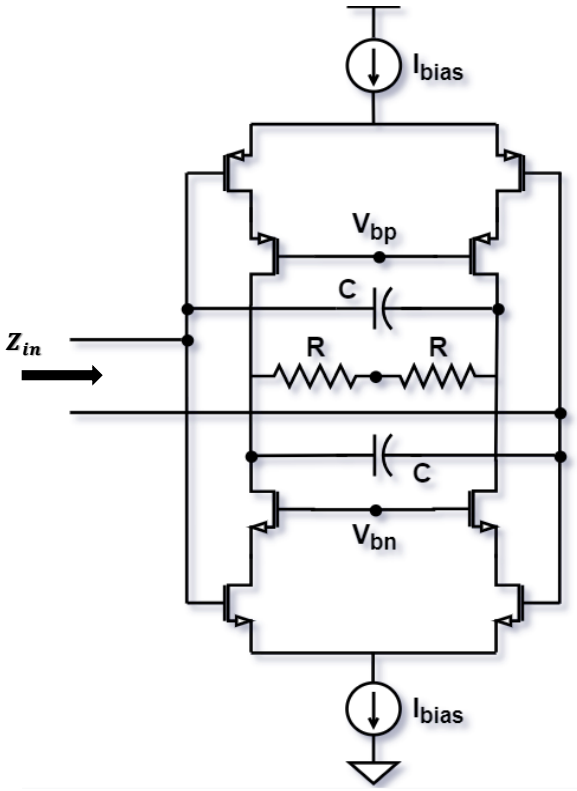

Figure 4: Miller negative capacitance.

From (eq.4), the single-ended input capacitance resulting as

$$C_{in} = (1 - g_m R)C. \tag{5}$$

The value of C is chosen so as to partially cancel the in-band positive input capacitance and it vanishes beyond the filter poles, causing the shunt capacitive impedance to increase around the ω_o. As a result, the poles Q is significantly increased.

The filter topology is shown in Figure 5. A stacked NMOS-PMOS (SNP) is chosen to avoid the noise of a tail current source. The CG stage ($M_{N,in}$,$M_{P,in}$) is biased through a diode-connected transistors ($M_{N,diode}$,$M_{P,diode}$).The diode-connected transistors size one-fifth of the CG stage and it follows that the DC current in CG is 5 times the current in diode-connected transistors. A

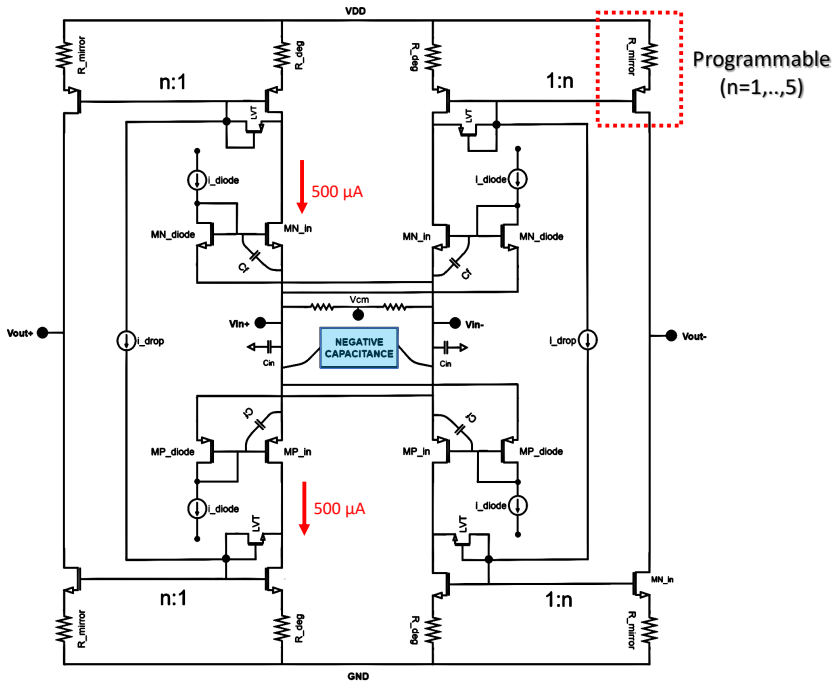

Figure 5: an open-loop biquad based on a regulated cascode architecture.

Parameter	Value
i_{diode}	100 μA
i_{drop}	10 μA
C_{in}	3 pF
R_{deg}	225 Ω
R_{mirror} (n=5)	45 Ω
$g_{m,MN_{in}}$	10 mS
$g_{m,MP_{in}}$	10 mS
$g_{m,MN_{diode}}$	2 mS
$g_{m,MP_{diode}}$	2 mS

Table 1: design parameters of the open-loop filter.

CMFB loop is used to set the DC voltage at the source of $M_{N,in}$, $M_{P,in}$ to $V_{dd}/2$. Design parameters are listed in Table 1. The output signal currents of SNP CG ($i_{outP,N}$) are recombined through two 1:n current mirrors, that are programmable (n=1,...,5). This gives a gain programmability of up to 14

dB. Moreover, the capacitor C_{in}, C_{neg} and C_f are also programmable, which gives the programmability of the bandwidth of the filter. The prototype is fabricated in TSMC 28 nm HPC technology (see Figure 6). The chip area is 1mm×1mm which contains an open-loop filter and a Rauch filter. The open loop filter area is 330μm×330μm.

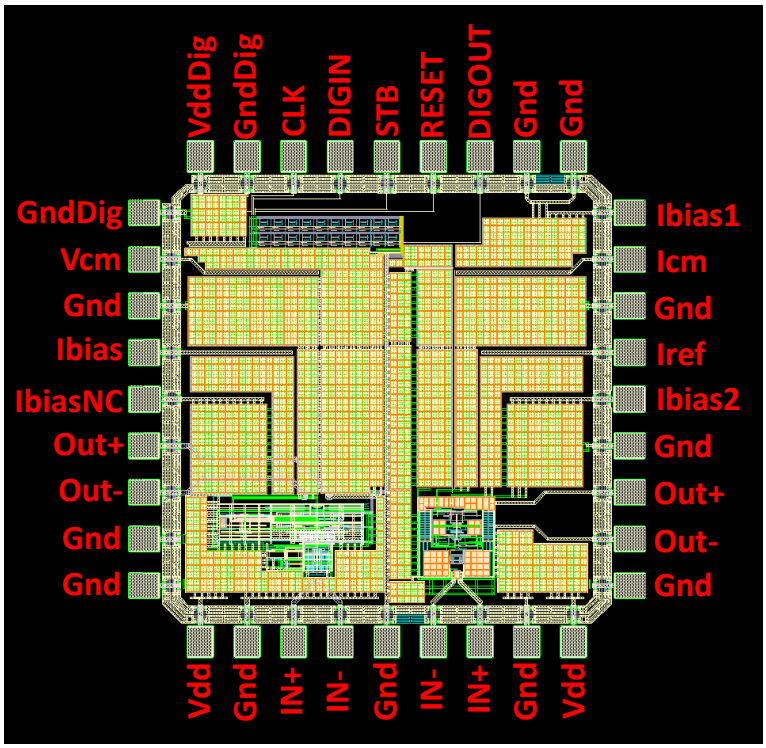

Figure 6: chip layout of the implemented open-loop filter.

SIMULATION RESULTS

The filter is simulated with different gain settings using the current mirror. The 14 dB gain variation is shown in Figure 7 and the bandwidth variation is shown in Figure 8, where the bandwidth can be varied from 650 MHz to 1050 MHz. The output noise integrated over a 1 GHz bandwidth is 1.28×10^{-7} V_{rms}^2 and the overall power consumption is 9 mW. The results summary is reported in Table 2.

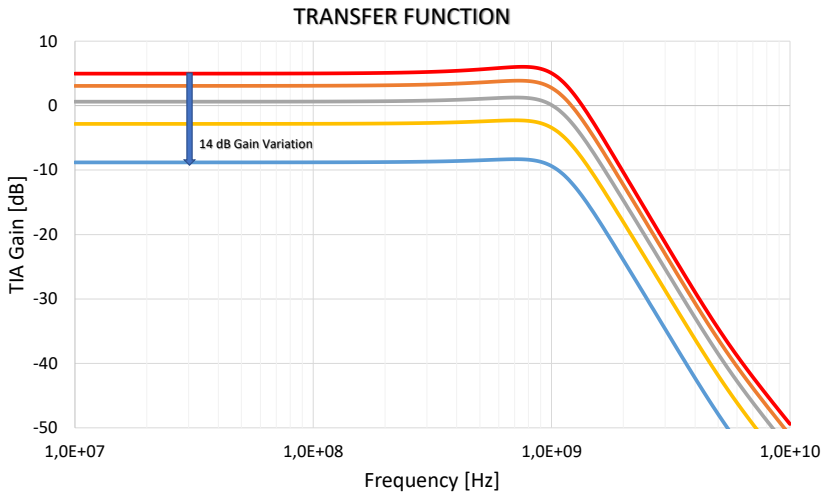

Figure 7: transfer function of the open loop filter with gain variation.

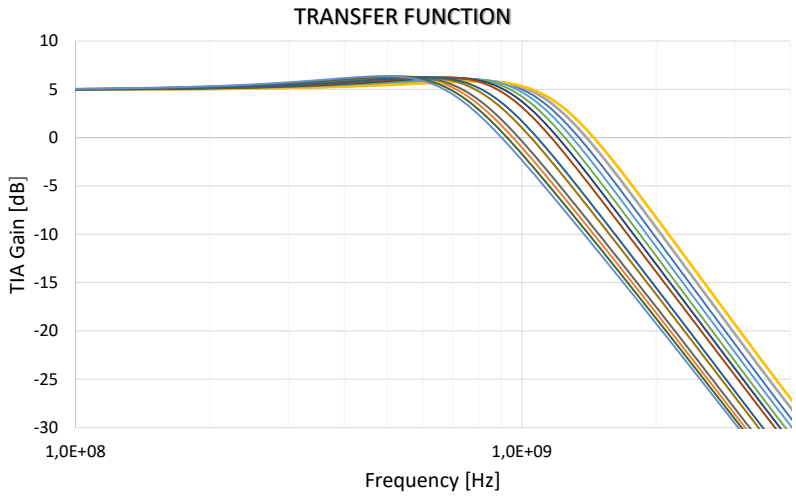

Figure 8: transfer function of the open loop filter with bandwidth variation.

Technology	cmos 28nm
P_{diss}	9 mW
Supply	1.5 V
f_c	1000 MHz
Order	2
OIP3	12.5 dBm
FOM	159 dBJ^{-1}

Table 2: summary of the simulated performance of the open loop filter.

The future activity will be concerned with the testing of the chip in the lab. A dedicated printed circuit board has been designed for the testing purposes. A long term plan will be the design of a full RX-chain in which the open loop filter will be incorporated.

Educational Activities

PhD Schools

- PhD School:"TOM2019 term-1", May 14^{th}-16^{th} 2019, Milan, Italy.
- PhD School:"SIE 2019", June 24^{th}-26^{th} 2019, Rome, Italy.
- PhD School:"TOM2019 term-2", September 10^{th}-12^{th} 2019, Milan, Italy.

Seminars

- 15^{th} November 2018, "Innovations in Big Companies", Speaker: Benedetto Vigna, President of the Analog, MEMS and Sensors Group STMicroelectronics. Organized by: Prof. E. Bonizzoni.
- 19^{th} December 2018, "Bosch Sensortec: MEMS sensors and ASIC Design for MEMS sensor", Speaker: Dr. Ivano Galdi, Analog IC Design Expert for consumers MEMS, at BOSCH Sensortec. Organized by: Prof. Andrea Mazzanti.

- 21st December 2018, "Radiation Detectors: Imaging What You Cannot See", Speaker: Prof. Cinzia Da Vi, University of Manchester, UK. Organized by: Prof. Lodovico Ratti.

- 21st December 2018, "Dynamic compression of the signal in charge sensitive amplifiers", Speaker: Prof. Massimo Manghisoni, Universit degli studi di Bergamo, Italy. Organized by: Prof. Lodovico Ratti.

- 14th January 2019, "Image sensors: challenges and applications", Speaker: Prof. Mohammad Azim Karami, Iran University of Science and Technology, Tehran. Organized by: Prof. Lodovico Ratti.

- 16th January 2019, "Extremely High Frequency Integrated Circuits for emerging communication networks", Speakers: Daniele Montanari, Federico Vecchi, Paolo Rossi and Maurizio Pagani. Organized by: Prof. Andrea Mazzanti.

- 15th April 2019, "eSilicon: Inroduction to DSP based Serial Links", Speakers: Matteo Pisati, Senior Manager at eSilicon and Feranado De Bernardinis. Organized by: Prof. Andrea Mazzanti.

- 6th May 2019, "A 64Gb/s Low-Power Transceiver for short - Reach PAM-4 Electrical", Speakers: Matteo Pisati, Senior Manager at eSilicon and Feranado De Bernardinis. Organized by: Prof. Andrea Mazzanti.

- 27th May 2019, "Catena: Bluetooth Transceivers", Speaker: Ugo Decanis, Senior rf-analog design engineer, at eSilicon. Organized by: Prof. Andrea Mazzanti.