UNIVERSITÀ DEGLI STUDI DI PAVIA
CORSO DI DOTTORANDO IN MICROELETTRONICA

PhD research activity 2017-2019

By: **Mahmoud Mahdipour Pirbazari**

Supervisor: **Andrea Mazzanti**

Academic year 2018/2019

Abstract

The report presents the research activities done during the second year of my PhD in the academic year 2018/2019. The research activities were in the framework of the DREAM project in which my main responsibility was providing local oscillation for a D-band radio enabling data rates up to 100Gb/s.

During this academic year, four main activities were done:

I. The first part of the frequency multiplier chain, a novel frequency tripler which was previously designed and sent for fabrication, was measured.
II. A second version of the previous chip was designed and sent for fabrication which included the previous tripler and also a new doubler and buffer. This chip, which up-converts the LO signal from X-band to E-band, will be used as a stand-alone frequency multiplier by 6 chip in the final demonstrator of the project.
III. A conference paper has been prepared based on the novelties of the tripler chip and accepted for publication in ESSCIRC 2019. Also a patent is prepared with STMicroelectronics and will be filed shortly.
IV. A frequency doubler chip was designed and sent for fabrication which up-converts its input LO from E-band to D-band. Measurements are expected in Q4 of 2019.

1. First frequency multiplier chip

The first frequency multiplier chip was designed during the first year of PhD and tested during the second year. This chip was meant to receive an input signal at X-band and up-convert it to E-band while comprising a tripler, a doubler and an output buffer. A novel tripler circuit was designed by the PhD student and the rest was done by a colleague. Figure 1-1 shows the overall architecture of this chip, referred to as “FMX6_A” from now on, fully designed and fabricated in STMicroelectronics 55nm BiCMOS technology.

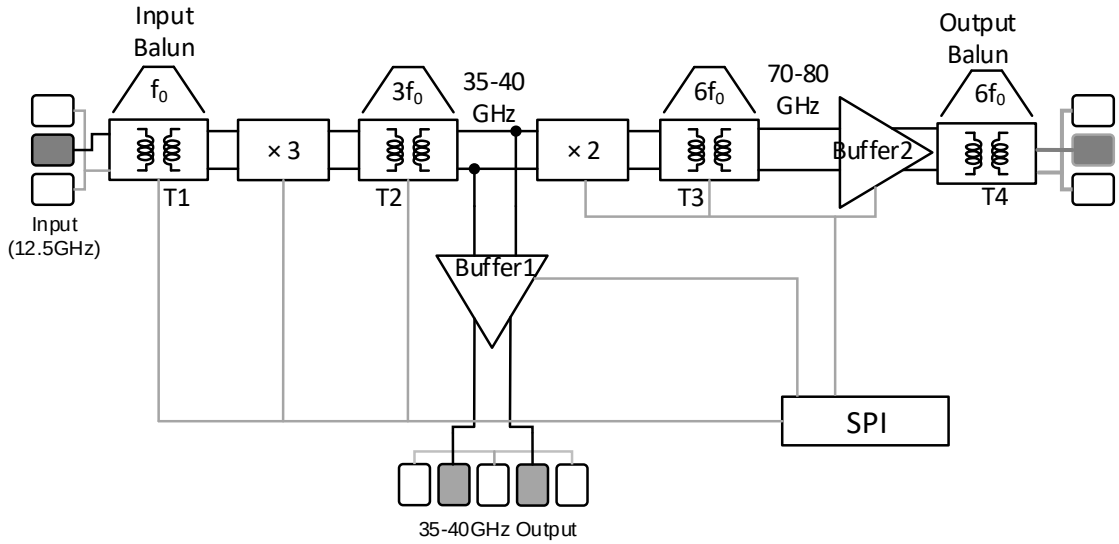

Figure 1-1. Overall architecture of the FMX6_A chip

In the following, results from measurement of the FMX6_A chip are presented. Figure *1-2* shows a photograph of the chip in which different blocks are marked. The chip measures 1.26mm by 0.81mm and there are 15 signal and supply pads, two GSG pads and one GSGSG pad.

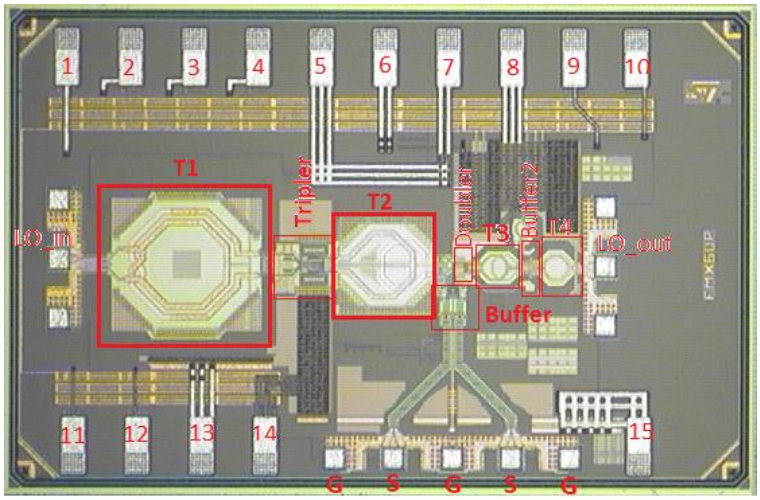

Figure 1-2. Photograph of the fabricated FMX6 chip

The tripler's output is tested using Buffer1 of Figure 1-1 which is connected to the dedicated GSGSG pad through transmission lines. This buffer is designed to achieve very wide band (allowing accurate measurements of spurious tones) and high linearity. Moreover, measurements are done single-ended, as differential probes were not available at this frequency. Figure 1-3 compares the measured and simulated power delivered to a 50Ω load at $3f_0$ and leakage of f_0 and $5f_0$ versus frequency when the tripler is driven by a 0dBm input signal. The single-ended peak output power is 0dBm at 37.8GHz and remains above -3dB variation from 35 to 41GHz, corresponding to 15.8% fractional bandwidth. Maximum and minimum rejection of f_0, $5f_0$ in this frequency range are 43.8dB and 37.5dB respectively. The tripler draws 13.6mA from a 1.7V supply while the output buffer, not optimized for power efficiency but for wide bandwidth and high linearity, draws 32mA from a 3V supply. From simulations, the differential voltage swing at the buffer's input is around 930mV zero-peak.

Figure 1-4 shows the measured output power at $3f_0$ when the input power is swept at 12.5GHz. The same plot reports the total Harmonic Rejection Ratio (HRR) considering signal leakage at f_0 and $5f_0$. In the range –5 to 10dBm the single-ended output power at $3f_0$ rises from -8 to +4dBm. The HRR remains better than 40dB until 4dBm input power and rises to 36.6dB for 10dBm input.

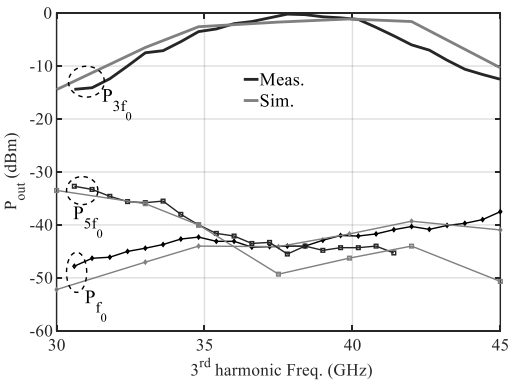

Figure 1-3. Measured output power of the 3rd harmonic, f_0, and f_5 leakage versus frequency for 0dBm input signal

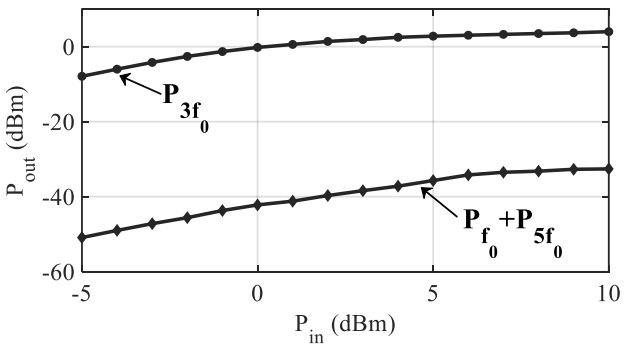

Figure 1-4. Measured output power of the 3rd harmonic and HRR versus input power at f_0=12.5GHz

Figure 1-5 shows input and output PN at 12.5GHz and 37.5GHz, respectively. The difference between the two plots is 9.5dB, as expected by the frequency multiplication by 3, thus proving negligible phase noise deterioration from the tripler.

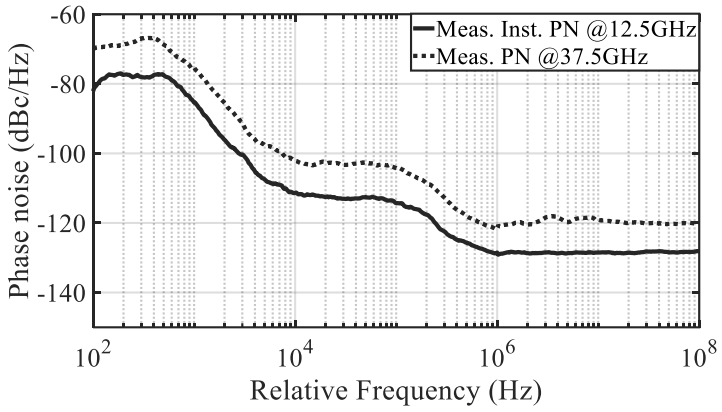

Figure 1-5. Phase noise performance.

2. Second frequency multiplier chip

In the second version of the frequency multiplier-by-6 chip, FMX6_B, the previous E-band doubler and buffer are redesigned by the PhD student. Figure 2-1 and Figure 2-2 show the designed doubler and output buffer, respectively. Figure 2-3 shows the layout of the FMX2 chip. The chip measures 1.71mm by 0.81mm and measurement are expected in Q2 of 2020.

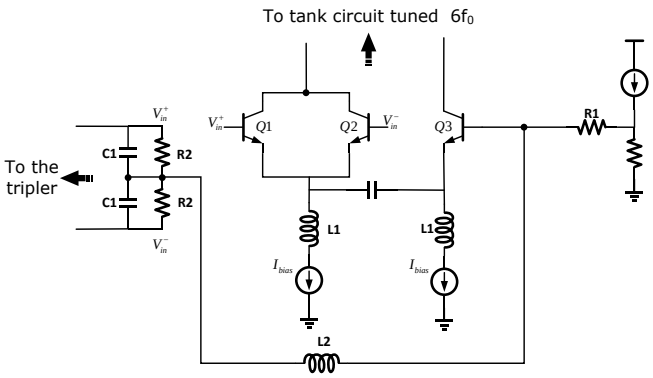

Figure 2-1. Modified E-band doubler

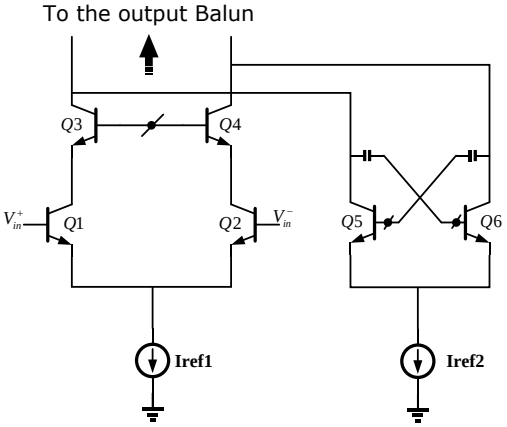

Figure 2-2. Output buffer using injection-locked technique

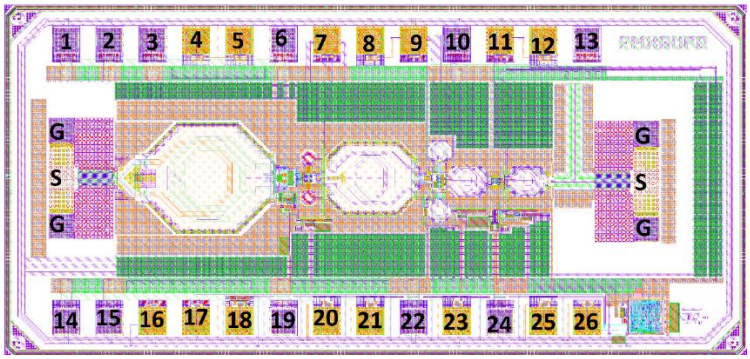

Figure 2-3. Layout of the FMX6_B chip

3. Third frequency multiplier chip

The D-band frequency doubler chip, FMX2, converts the input E-Band signal up to D-band (150GHz centre frequency). Figure 3-1 shows the overall architecture of the FMX2 chip, fully designed in STMicroelectronics BiCMOS55nm technology. Figure 3-2 shows the layout of the FMX2 chip. The chip measures 1.08mm by 1.08mm.

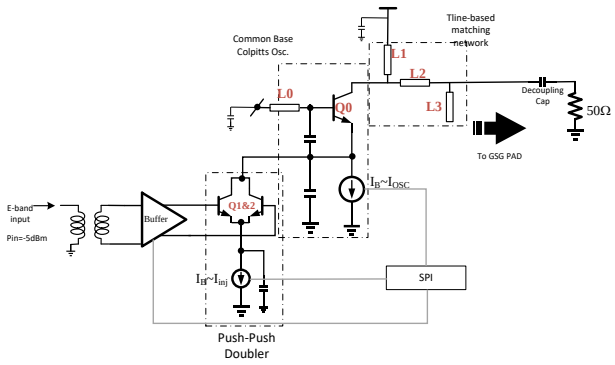

Figure 3-1. Overall architecture of the FMX2 chip

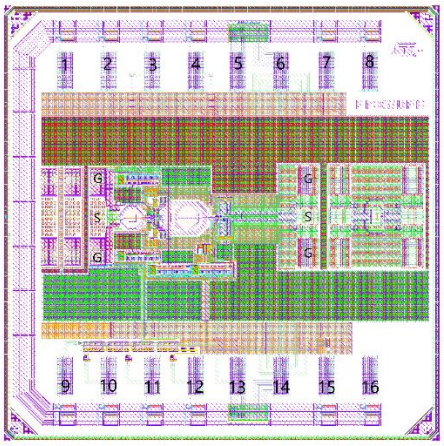

Figure 3-2. Layout of the FMX2 chip with pad numbers

Different aspects of the FMX2 chip have been investigated and the most relevant results of post layout simulations are presented in this section. The whole chip consumes 64.5mW of which 7.6mW is consumed by the bias circuits. Figure 3-3 shows output power of the chip for a -5dBm input power from the input LO source versus frequency. Power at $2f_0$ (the frequency of interest) is plotted with respect to a 50Ω reference. Figure 3-4 shows the output power at $2f_0$ for three different frequencies , when the input power is swept from -15dBm to -5dBm

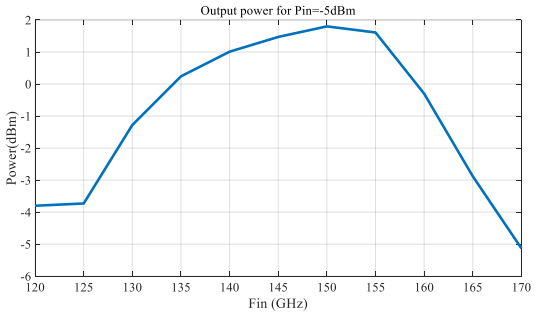

Figure 3-3. Output power versus frequency for -5dBm input (reference is 50Ω)

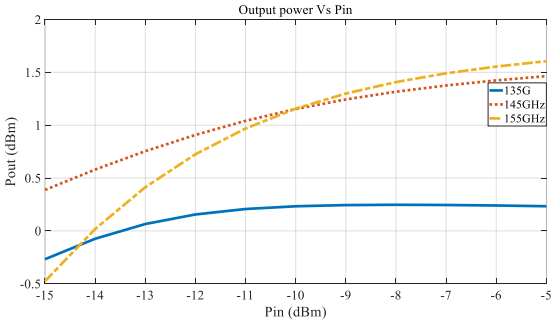

Figure 3-4. Output power vs input power at 135, 145, and 155GHz

The chip has been sent for fabrication and measurements are expected to be carried out in the fourth quarter of 2019.

Credits

Seminars attended:

No.	Seminar title	Date	credit
1	Facebook: Advanced RF Front-End & Transceiver Systems Design Overview for Carrier Aggregation based 4G/5G Radios	October 1st 2018	0.2
2	AMS: Magnetic and Inductive Position Sensors for Industrial and Automotive Applications	October 28th 2018	0.2
3	STMicroelectronics: Innovation in Big Companies	November 15th 2018	0.2
4	GT: Bayesian Framework for Optimization of Structures in Microsystems Integration	December 5th 2018	0.2
5	Bosch Sensortec: Company Overview, MEMS sensors And ASIC Design for MEMS sensor	January 9th 2019	0.2
6	Dr. Karami: Image sensors: challenges and applications	January 14th 2019	0.2
7	Huawei: Extremely High Frequency Integrated Circuits for Emerging Communication Networks	January 16th 2019	0.2
8	On-Chip Epilepsy Detection: Where Machine Learning Meets Personalized Wearable (IEEE continuing education)	January 24th 2019	0.2
9	Infineon: Advances in Power Management for Automotive Applications	March 18th 2019	0.2
10	eSilicon: Introduction to DSP based Serial Links	April 15th 2019	0.2
11	Catena: Bluetooth Transceivers	May 27th 2019	0.2

Graduate course:

No.	Course title	credits
1	RF microelectronics	9

PhD school, intensive course:

No.	School name	credits
1	TOM2019/1	3.5
2	Fundamental Concepts in Jitter and Phase Noise, ESSCIRC2019 tutorials	1.3

Publication and presentations:

No.	Publication /Congress	credits
1	One Publication in ESSCIRC2019, Krokow, Poland (one PhD student)	2
2	One Presentation in ESSCIRC2019, Krokow, Poland	1
3	PhD annual presentation	0.5

Summary of credits	2018/2019 academic year	19.5
	total	22.4