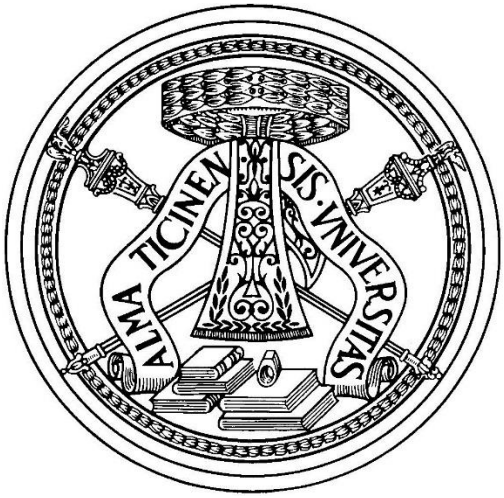
# UNIVERSITY OF PAVIA




## Ph.D. Second Year

## Report

High Speed Wireline Receiver Front-end

And

D-Band Amplifier Design and Measurement

Ibrahim Petricli

Supervisor: Andrea Mazzanti

The activity of second year can be divided into two parts, first part was continuation of my master thesis project titled “ Analysis and Design of a 56 Gb/s PAM4 Un-Clocked Decision Feedback Equalizer in 16 nm FinFET”. The activity held by collaboration with STMicroelectronics and it has been decided to be improved. The aim of the activity is to increase the datarate to 112 Gb/s (2 times of the previous work) and to port the design from 16nm FinFET to 7nm FinFET.

First step was to increase the speed. In order to do that all sub-blocks in the design were redesigned. Since the main difference is datarate, bandwidth of all blocks were increased to avoid introducing ISI to the signal. In the previous design to have high bandwidth, shunt peaking method was used. In order to increase further, peaking inductors were replaced by T-Coils. And also bias points were optimized in order to get maximum performance of the technology. Un-clocked DFE loop comprises 3 main blocks; Adder, Threshold and Delay. Beside bandwidth optimization to avoid ISI, also the delay contribution of each block has to be considered and optimized accordingly.

Second step was to port design 16nm FinFET to 7nm FinFET. The main difference between 2 technology was optimum current density for transistors. Also post layout parasitic contribution is different for two technology. Therefore 7nm design was re-optimized considering those aspects. In addition to these changes, there was a system level difference between 7nm design and thesis work. In the thesis, the UCDFE has 2 tap correction. 1st tap was correcting 1st and 2nd tap was correcting 2nd post cursor. As a difference the 2nd tap replaced by IIR feedback. So not only 2nd post cursor was removed but also further improvement has succeded. The output eye diagram of the final design is shown in Figure 1. The vertical eye opening is %14 and horizontal eye is 0.45UI.

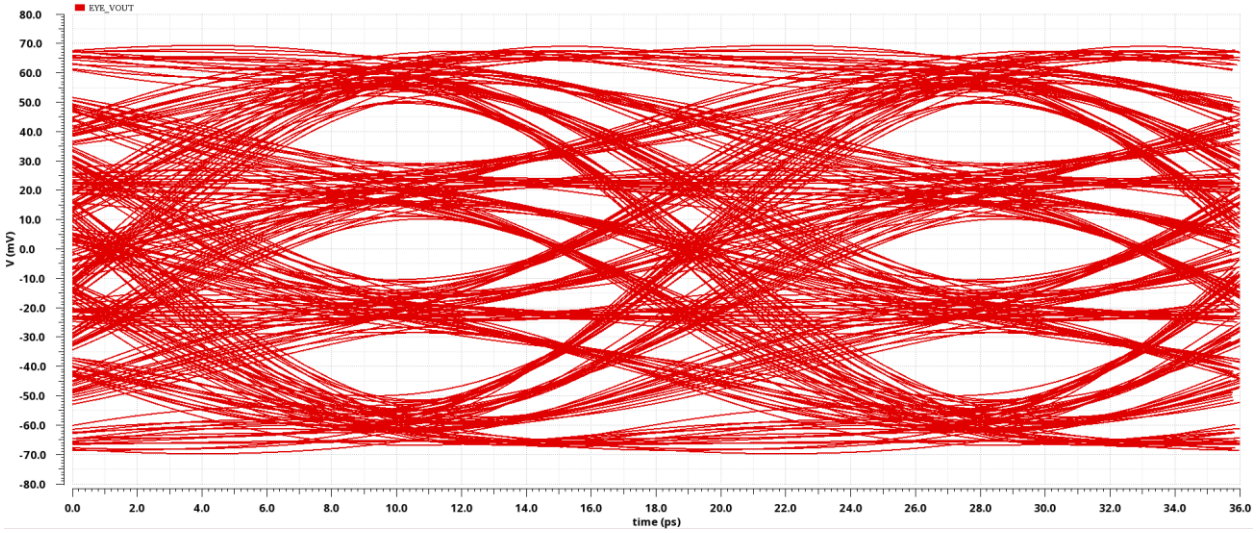



Figure 1: Eye Diagram of UCDFE Output

The second part of the activity was related to design of D-Band building blocks. In the first year simple amplifiers were designed and tape-outed in order to assess BiCMOS 55nm technology in D-Band. As a continuation, after the chip has received, I have completed the measurements. In order to characterize device parameters in PDK, also standalone devices such as BJT, transmission lines and capacitors were placed on the chip and measured on the probe station. The layout and the microphoto of the chip are shown in Figure 2.

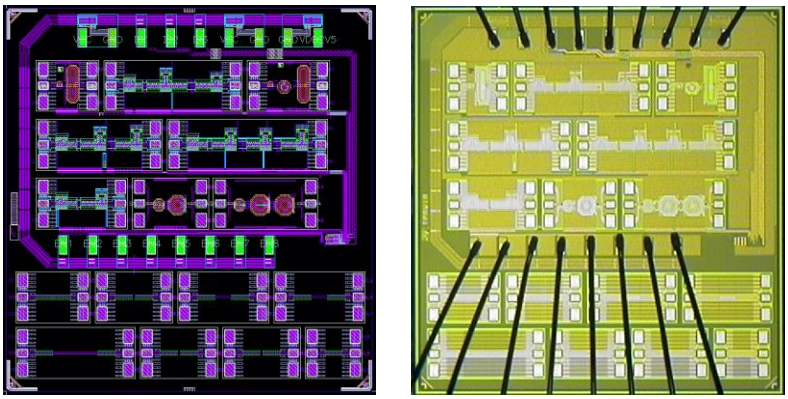


Figure 2: Layout and Chip Microphoto

In the following figures S-parameters of 4 amplifiers are shown. As seen from figures measurement results are well aligned with the simulation results.

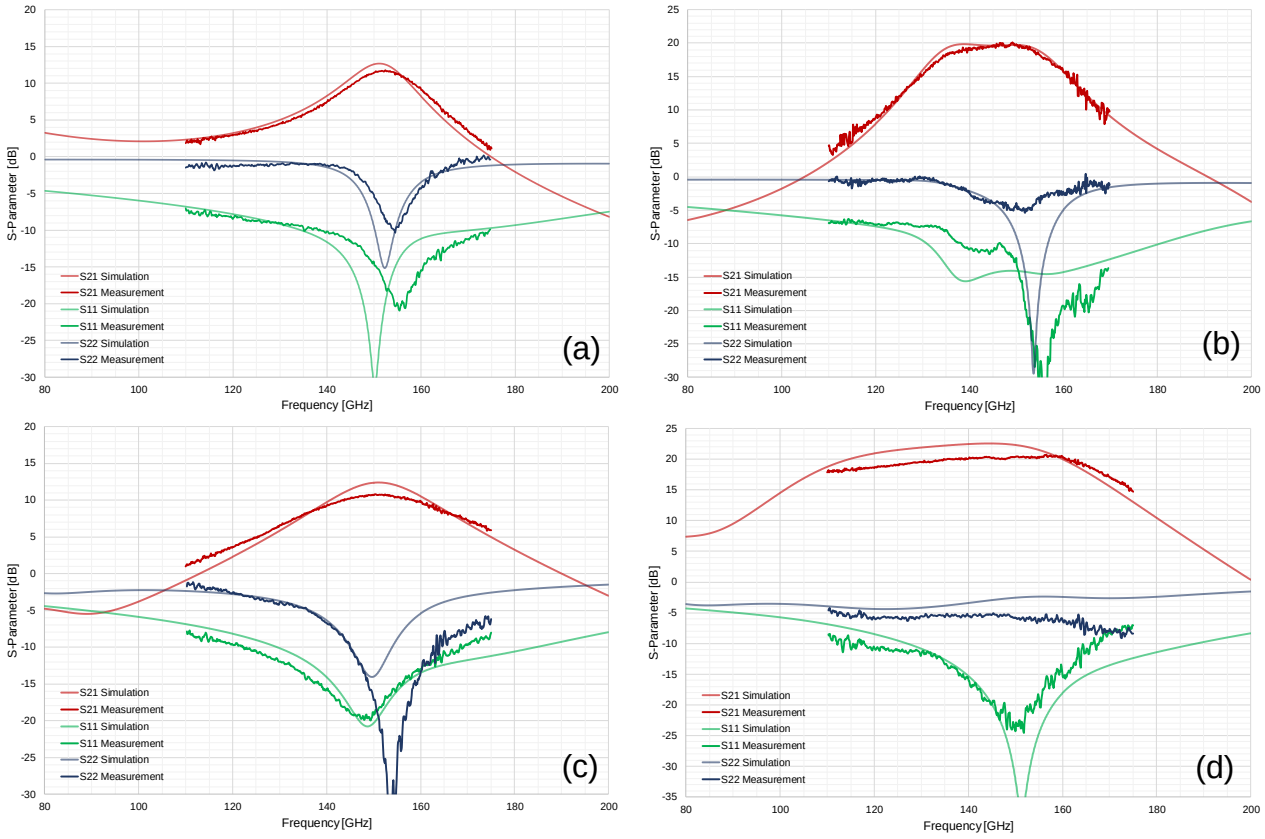



Figure 3: S-Parameter of 1 and 2 Stage Amplifiers with Lumped Element (a,b) and T-Line Matching (c,d)

Beside adopting design methodology and technology assessment, the scope of the activity is defined by TARANTO European project which is to design D-Band extension module. Therefore, in this activity my part was to design power amplifiers. To accomplish the task, I have designed 1 single ended and 1 differential power amplifier in 2 different technologies i.e. BiCMOS55 and BiCMOS55+. All designs are 4 stages. Differential designs were optimized by re-using single ended amplifier cores. Schematic and layout of single ended and differential designs are shown in Figure 4 and Figure 5.

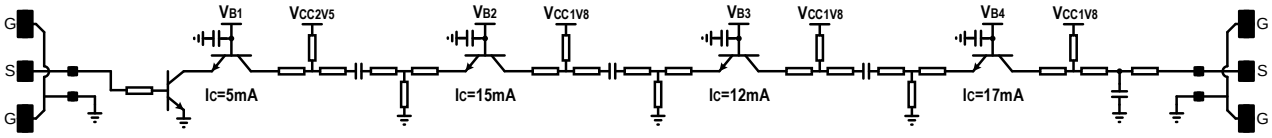



Figure 4a: Schematic of Bi55 Single Ended Amplifier

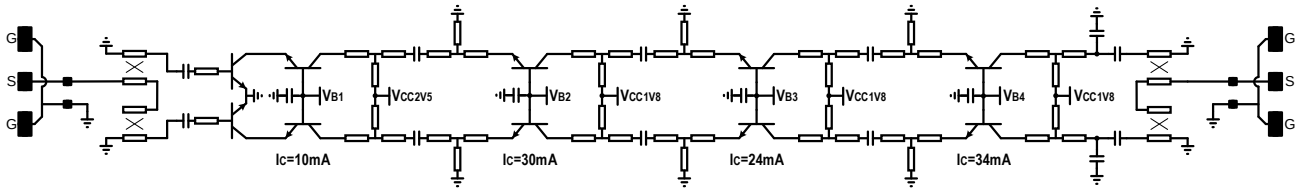



Figure 4b: Schematic of Bi55 Differential Amplifier

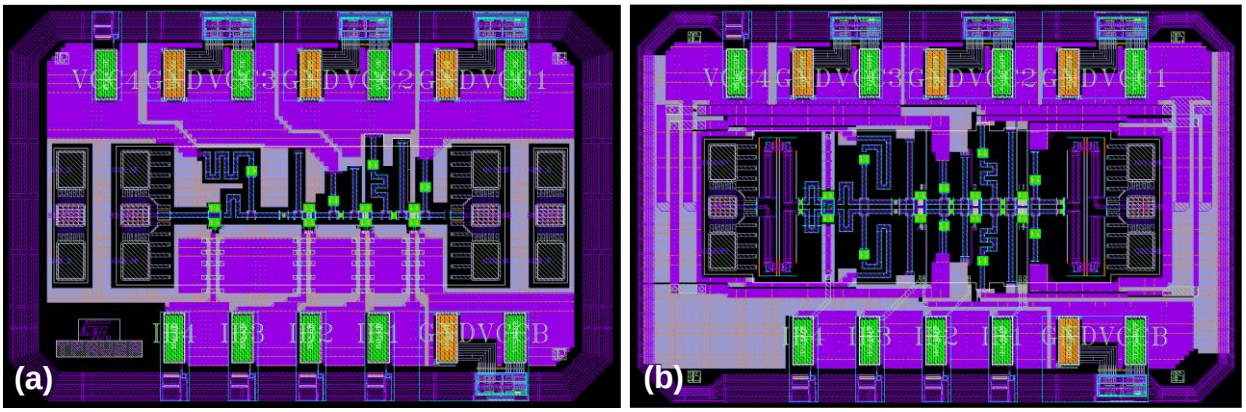



Figure 5: Layout of Bi55 Single Ended (a) and Differential Amplifier (b)

Post layout simulation results are shown in Table 1.

| | GP [dB] | BW [GHz] | OP1dB [dBm] | Psat [dBm] | PAEmax [%] |
|---|---|---|---|---|---|
| Bi55 Single Ended | 24.6 | 33.1 | 14.3 | 16.2 | 13.8 |
| Bi55 Differential | 22.5 | 32.1 | 16.1 | 17.9 | 10.5 |
| Bi55+ Single Ended | 31.0 | 31.9 | 14.1 | 15.3 | 12.9 |
| Bi55+ Differential | 29.3 | 26.2 | 16.1 | 17.4 | 10.2 |

Table 1: Performance Summary