UNIVERSITÀ DEGLI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

Activity report a.a. 2017/2018/2019

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Ciclo: XXXIII

Scientific activity

IIP2 improvement technique for an inductor-less TVWS LNTA receiver

In the last years the research activity has been strongly pushed to find new and original solutions for high frequency receivers. The underlying reason is need for improved spectral efficiency imposed by 4G and the emerging 5G standards, especially in the range of frequencies up to 6GHz. The TV band, which ranges from 54 MHz to 862MHz, is currently underutilized and there has been a strong push to use part of it for mobile communications. The so-called TV White Space (TVWS) is represented by the portion of the TV spectrum that are not used. In order to take advantage of the TVWS it is required to sense all the bands and to detect the unused portions of it, which can be used for sending and receiving data. This concept is called "Cognitive Radio". Another issue of TVWS and, more in general, of future sub-6GHz 5G transceivers, is the interference problems, given the very high relative input bandwidth. Unfortunately, the classic solution based on Surface Acoustic Wave (SAW) filters cannot be used because SAW fiters are difficult to tune and have finite bandwidth. Consequently, they are not suitable for Cognitive Radio applications where the center frequency and bandwidth change continuously with the time. Moreover, the presence of a wideband balun at the receiver input is not recommended being bulky, expensive and lossy.

One of the often underestimated challenges, for a SAW-less and wideband receiver, is the second order non linearity. In fact, two or more interferers can create second-order intermodulation spurious tones which can fall in-band, deteriorating the original signal. Consequently, the receiver for a TVWS application must have a large bandwidth (more than 1 decade) and high linearity, both in terms of IIP2 and IIP3.

In order to have high IIP2, a differential receiver is to be preferred. A possible solution to avoid the use of an external balun is the single-ended input, differential output Low Noise Transconductance Amplifier (LNTA). The LNTA output current can be down-converted through a current-mode passive mixer and transformed back to voltage thanks to baseband (BB) Trans-Impedance Amplifier (BB-TIA). This solution provides low power consumption and high linearity.

The LNTA needs large bandwidth, low noise, input impedance matching and high linearity. A possible solution is given by the noise-cancelling LNTA [1], which uses a pair of Common Gate (CG) and Common Source (CS) amplifiers. The CG provides the desired input impedance, fulfilling the matching condition, while the CS provides a second gain path that cancels out the noise and distortion introduced by the CG. In order to achieve a fully balanced output a current mirror can be used at the output of the CG, allowing to remove the input balun, as shown in Fig.1 [2].

In [2] both PMOS and NMOS transistors are used in the CG and CS stages. In this configuration, another distortion cancellation mechanism can be exploited. Indeed, as explained in [3], the PMOS and NMOS devices have opposite 2^{nd} order coefficients, which can result in a very high IIP2. This cancellation, however, is very sensitive to device biasing and size. As a result, the reported solutions are not robust to PVT variations. The work carried out during this first year was to develop an algorithm that can automatically find the correct bias and device width for minimizing the 2^{nd} order distortion.

The idea is to detect the minimum in the 2^{nd} order distortion of the CS output current by measuring its DC component. Considering a target IIP2 of 40dbm, an input signal of 100mV and a transconductance of 20mS, the minimum DC 2^{nd} order current (I_{2dc}) that must be detected is 5uA. This DC component is superimposed to a large signal. To overcome this problem, during the IIP2 calibration phase, the LNTA CS-side is connected to a passive low-pass filter and the measurement is carried out with a simple filtering comparator. Based on the comparator output the PMOS device of the CS stage and its bias current are adjusted. The complete algorithm procedure is explained in Fig.2. The chip has been integrated in a 28nm CMOS technology and is currently under test.

Analysis and design of a transceiver for Full-Duplex applications

The Full-Duplex theory wants to merge together two of the most important methods for transmitting data, the Time Division Duplexing (TDD) and the Frequency Division Duplexing (FDD). Indeed, this kind of transceiver would transmit and receive at the same time using the same band, increasing the spectrum efficiency of a factor of two. Despite this solution is promising, it must face out a lot of challenges. The most stringent one is due to the transmitter echo. Indeed, the transmitter can manage power in the order of 25/30 dBm while, the receiver, has to sense small powers around -80/-90 dBm. The key point is to cancel out the transmitter echo for not bring in saturation region the receiver, and to reduce its power until its contribution is comparable to the receiver noise. The solution proposed is shown in Fig.3 and forecast 3 stages of cancellation. The first one exploits an auxiliary receiver for sensing the transmitted signal together with its noise and distortion. Then, in digital domain, their contributions are cancelled. The second one, uses a hybrid transformer for mitigate the transmitter power that passes through the receiver, Fig.4. In fact, this passive component is a 4 ports network connected to: antenna, receiver, transmitter and balancing nodes, respectively. The balancing is, simply, a node connected to a variable impedance that tries to copy the antenna one. Once this condition is met, the transmitter is electrically disconnected to the receiver path. Obviously, it is not

possible to cover all the possible values for all the RF bandwidth. Therefore, only 40 dB of cancellation is considered a reasonable target. The solution adopted to design the balancing network is a CLC network with one node connected to an high-linear external 50Ω, Fig.5. Each variable device exploits a 2:1 transformer ratio. In this way, the input voltage is attenuated, making easier to design the variable impedance that must manage high powers. The third stage of attenuation is exploited in baseband using a local feedback. A digital I/Q complex filter is used to compare: the original data of the transmitter and the output echo. Thanks to this comparison, the digital filter computes the correct coefficients that are given to the DAC for cancel it. In a different way, the digital filter determines the impulse response of the entire transceiver path for compute an extra cancellation in baseband. With all these three cancellations, the transmitter echo is cancelled for more than 110dB. The auxiliary receiver exploits a single ended to differential transformer for getting an attenuation of 40 dB at the input. Then, the receiver is a simple mixer 1st topology with high in-band linearity. The main receiver employs a high-linear LNTA as first stage concluding with the same topology of the auxiliary receiver. The baseband bandwidth is equal to 40MHz for both the receivers. The gain, NF and IB-IIP3 are 32.5dB,7dB and 22 dBm, respectively. The chip has been designed in tmsc28 and is currently under test.

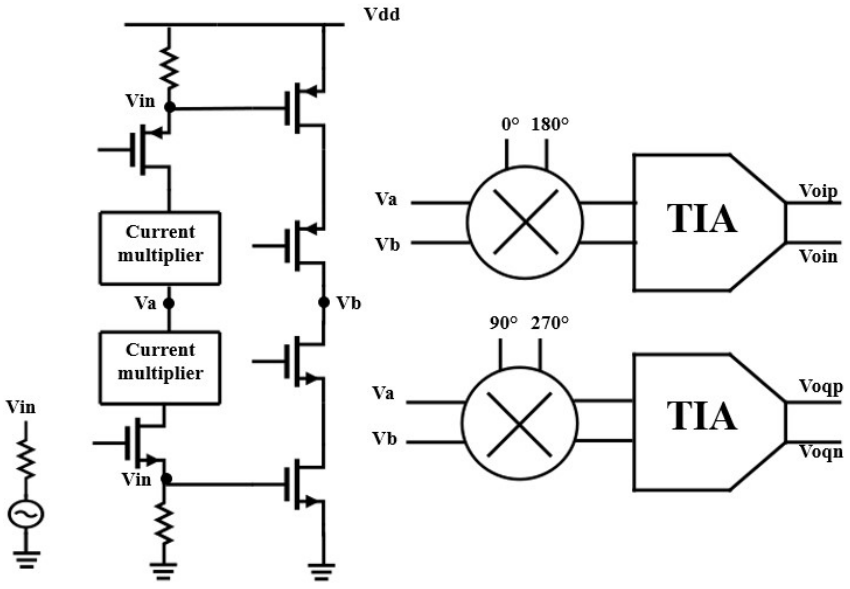

Fig.1, Simplified schematic of the noise-cancelling CS-CG amplifier.

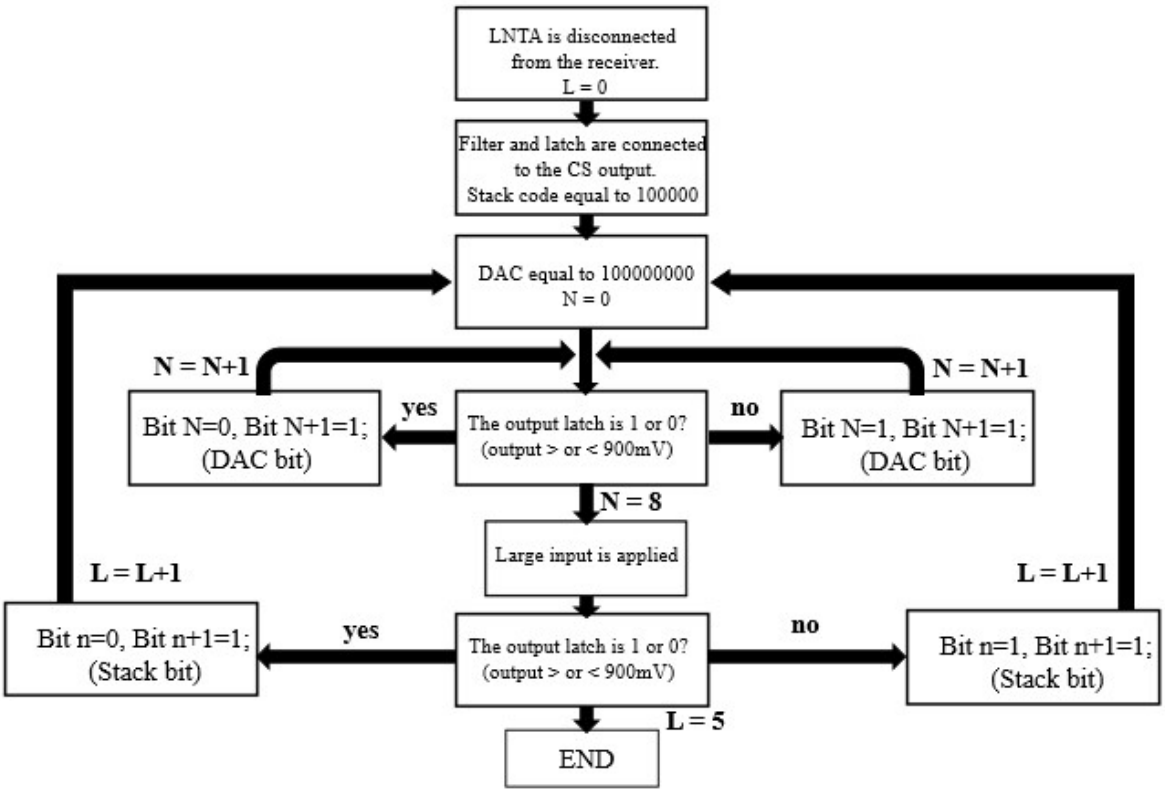

Fig.2 Algorithm flowchart.

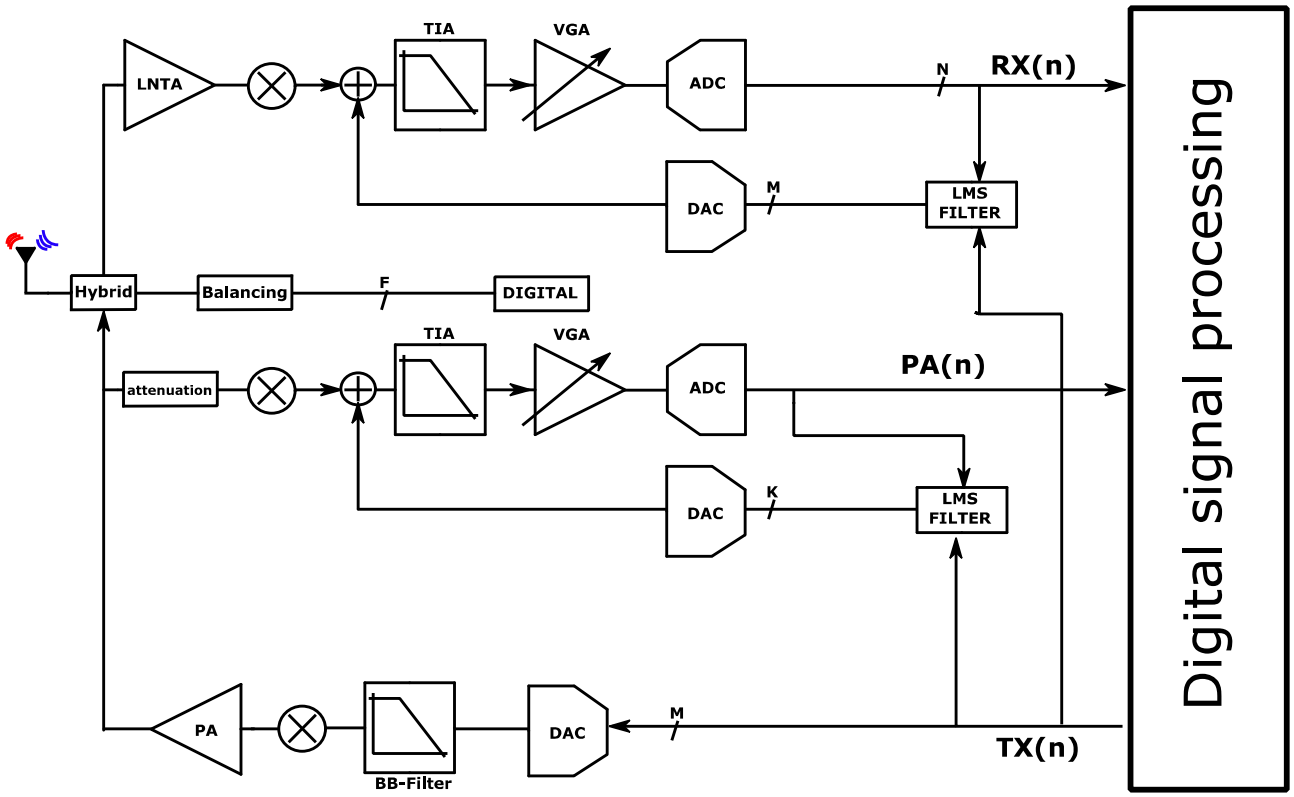

Fig.3 Proposal solution for a Full-Duplex receiver

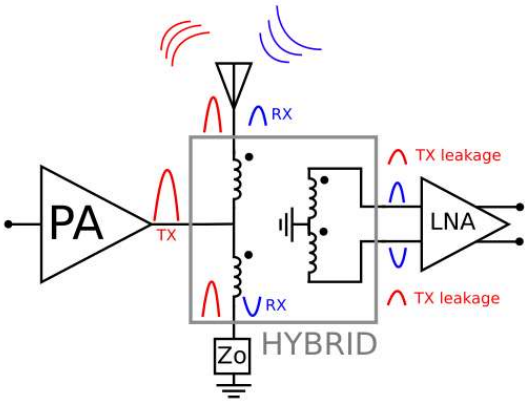

Fig.4 The hybrid transformer.

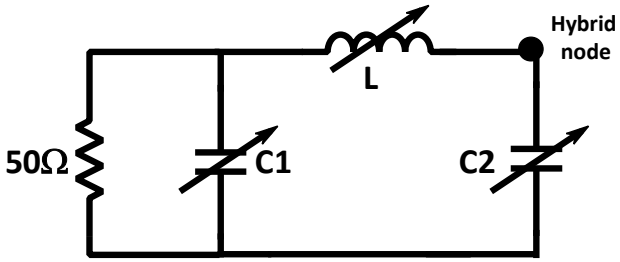

Fig.5 The Balancing network.

Seminars attended

First year

- 18/10/17 – *"Bosh sensortec: company overview, MEMS sensors and ASIC design for MEMS sensors"*, organized by Prof. A. Mazzanti.
- 20/11/17 – *"Dynamic interactions in smart electronic power distribution system"*, organized by Prof. N. Anglani.
- 22/11/17 – *"Maxim Integrated: DC-DC converter overview"*, organized by Prof. A. Mazzanti.
- 6/12/17 – *"High frequency integrated circuits for SG and high speed optical transmission"*, organized by Prof. A. Mazzanti.
- 13/12/17 – *"AMS: Chip design for automotive applications and layout guideline for ESD/LU robustness"*, organized by Prof. A. Mazzanti.
- 10/1/18 – *"Silicon photonics electro-optical transceiver front-ends"*, organized by Prof. A. Mazzanti.
- 17/1/18 – *"Emerging memories: design techniques for improved reliability and scaling"*, organized by Prof. A. Mazzanti.
- 18/1/18 – *"From SPAD to quantum computers"*, organized by Prof. S. Donati.
- 29/1/18 – *"Reheasal of presentations for the upcoming ISSCC"*, organized by Prof. A. Mazzanti and Prof. E. Bonizzoni
- 16/2/18 – *"Antenna design and integration for nanotechnology based sensor nodes"*, organized by Prof. M. Bozzi.
- 26/3/18 – *"E-silicon meets Pavia University"*, organized by Prof. A. Mazzanti.

- 25/5/18 – *"Millimeter-wave measurements using converter-based vector network analyser system"*, organized by Prof. M. Pasian.
- 1/6/18 – *"Dissecting design choices for power efficient continuous-time Delta Sigma Analog- To-Digital converters"*, organized by Prof. E. Bonizzoni.
- 4/6/18 – *"On-chip active delay lines with widely tunable delays"*, organized by Prof. D. Manstretta.

Second year

- 1/10/18 – *"Advanced RF Front-End & Transceiver systems design overview for carrier aggregation based 4G/5G radios"*, organized by Prof. Manstretta.
- 23/10/18 – *"AMS: Magnetic and inductive position sensors for industrial and automotive applications"*, organized by Prof. Bonizzoni.
- 15/11/18 – *"Innovation in big companies"*, organized by Prof. Bonizzoni.
- 5/12/18 – *"Bayesian framework for optimization of structures in microsystems integration"*, organized by Prof. Bozzi.
- 21/12/18 – *"Radiation detectors: Imaging what you cannot see"*, organized by Prof. Ratti.
- 21/12/18 – *"Dynamic compression of the signal in charge sensitive amplifiers"*, organized by Prof. Ratti.
- 14/01/19 – *"Image sensors: Challenges and applications"*, organized by Prof. Ratti.
- 16/01/19 – *"Extremely high frequency integrated circuits for emerging communication network"*, organized by Prof. Mazzanti.
- 27/05/19 – *"Catena Bluetooth transceiver"*, organized by Prof. Mazzanti.
- 06/06/19 – *"Wavelenght switching technologies and coherent systems design in photonic backbones"*, organized by Prof. Lodi.

Attendance to schools

First year

- Ph.D Course: *"Topics on Microelectronics"*, March (9^{th}, 11^{th}) 2018, University of Milano-Bicocca, Milan, Italy.
- Ph.D Course: *"Essay Writing Techniques"*, December 14^{th} 2017 and January 18th 2018, Università degli Studi di Pavia, Pavia, Italy. Speaker: Prof. Hugo de Jonge.

Second year

- Ph.D Course: *"Topics on Microelectronics"*, September (18^{th}, 20^{th}) 2018, University of Milano-Bicocca, Milan, Italy.

- Ph.D Course: *"Topics on Microelectronics"*, May (14^{th}, 16^{th}) 2018, University of Milano-Bicocca, Milan, Italy.
- Ph.D Course: *"SIE 2019"*, June (24^{th}, 26^{th}) 2019, University of Torvergata, Rome, Italy.

Pubblications

- Paper Title: *"A Mixer-1^{st} auxiliary receiver for Full-Duplex self-interference cancellation"*, November (19^{th}, 20^{th}) 2018, New Generation CAS, Valletta, Malta.
- Poster Title: *"Analysis and design of a Mixer-First receiver for Full-Duplex self-interference cancellation"*, June (24^{th}, 26^{th}) 2019, SIE, Rome, Italy.

References

[1] Stephan C. Blaakmeer, Eric A. Klumperink, Domine M.W. Leenaerts, Bram Nauta, "Wideband Balun-LNA With Simultaneous Output Balacing,Noise-Canceling and Distortion-Canceling", IEEE Journal of Solid-State Circuits, vol. 43, No.6, June 2008.

[2] *"A TVWS LNTA with Balanced Output Employing a Low-Noise Current Multiplier"* at 13^{th} Conference on PhD Research in Microelectronics and Electronics (PRIME), June 12^{th}-15^{th}, 2017, Giardini Naxos - Taormina, Italy;

[3] Heng Zhang, Edgar Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifires: a Tutorial", IEEE Transaction on Circuits and System, vol.58, No.1, January 2011