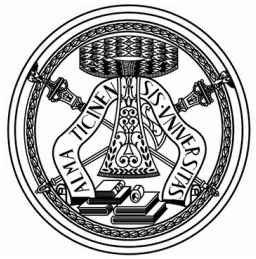

UNIVERSITA' DI PAVIA

UNIVERSITÁ DELGI STUDI DI PAVIA

CORSO DI DOTTORATO IN MICROELETTRONICA

An Extended Range Incremental Sigma-Delta ADC Design

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INTRODUCTION

Analog-to-Digital converters (ADCs) used in automotive applications often require very high absolute accuracy and linearity, as well as very low offset and noise with low power consumption. The properties of incremental A/D converters (IDCs) are well matched to the automotive requirements. They provide very precise conversion with accurate gain, high linearity, and low offset, and the conversion time can be relatively short. The key property of these converters is that they do not rely on precisely matched analog elements to achieve high resolution, but on oversampling, noise-shaping, and digital post-filtering. Thus, these converters can be integrated well into todays fine line-width CMOS technologies. The ADC proposed is targeted to achieve an effective number of bits (ENOB) equal to 12 at a clock frequency of 80 MHz, with a conversion time lower than 25 clock cycles. Specialized digital decimating filters are also described for such converters.

INCREMENTAL SIGMA-DELTA MODULATOR

The SAR ADC approach has limitations meeting these requirements. Hence, the alternative is to contemplate about a hybrid architecture. Since, the specified requirements are in line with the characteristic of the ISDM, thus a productive alternative.

Modified Feedforward Architecture of Second Order Incremental ΣΔ Modulator:

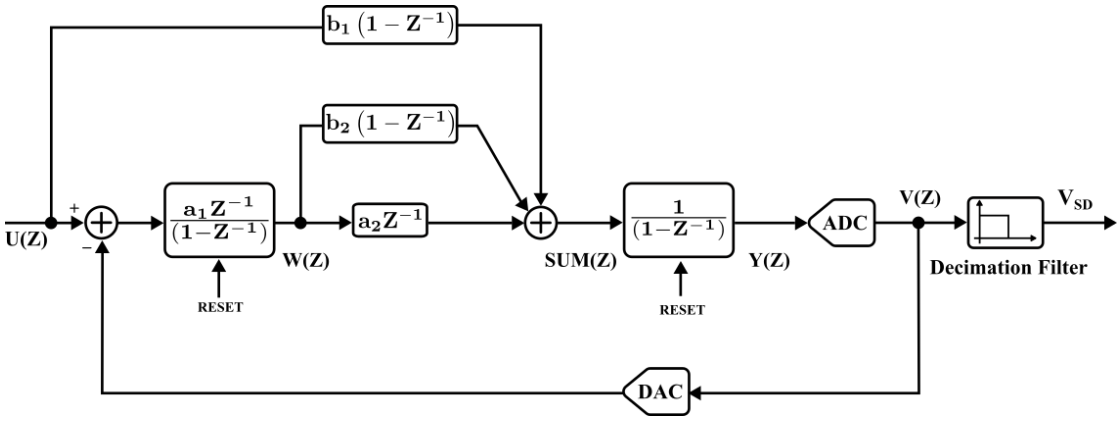

Fig. 2.1 Second Order Incremental Modified Feed-forward Architecture of Sigma-Delta Modulator

Fundamentals:

The block diagram of the second order IΣΔM is shown in Fig. 2.1. This structure is consists of two integrators followed by a multi-bit quantizer and a feedback DAC. In order to reuse the same hardware to digitize more than one analog input signals, reset feature is incorporated in modulator, hence the name Incremental Sigma-Delta Modulator. The structure is reset at the beginning of the new conversion cycle including

analog and digital memory elements. Then sample is acquired using sample and hold circuit and is applied to the structure for conversion.

Provided that the oversampling ratio M is high enough, the reconstruction can be achieved by passing the output signal through a decimation filter with down sampling by a factor of M i.e. OSR. Thus output can be represented as in Eq 2.1.

$$V_{SD} = \frac{2a_1a_2}{2b_1 + a_1a_2M(M-1)} V_{ref} \left(v[M-2] + ... + (M-1)v[0]\right) \tag{2.1}$$

Where V_{SD} represents the digital equivalent of the input sample.

For multi-bit quantizer, considering second order loop filter with oversampling ratio of M, the obtainable effective number of bits (ENOB) can be expressed approximately as,

$$ENOB = N_{SD} + 2\log_2(M) - 2 \tag{2.2}$$

where, N_{SD} is the resolution of the quantizer used in ΣΔ loop and M is the over sampling ratio.

EXTENDED RANGE INCREMENTAL SIGMA-DELTA MODULATOR

The resolution of an IΣΔ modulator can be improved over that obtained with the simple decimation described above in Eq. 2.2 by using an estimate of the residual error V_{RS} to reduce the quantization noise at the output of the modulator order modulators, and higher-order modulators, where the residue of the modulation is the difference of output of the second integrator, output of first integrator. Shown in Fig. 3.1 is the block modulator with extended range diagram of a second-order IΣΔ modulator with extended range. Through this path of gain block and the quantizer, the residue is passed and it's

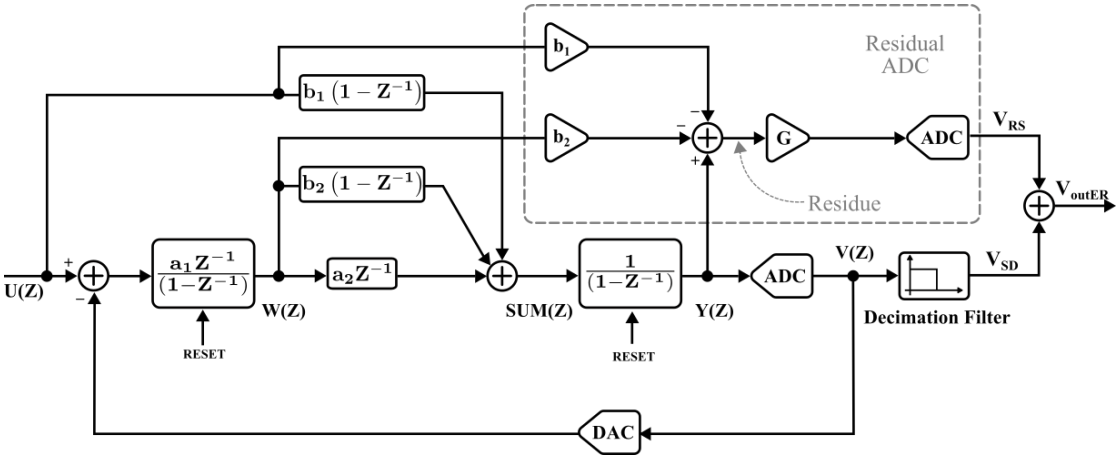

Fig. 3.1 Extended Range Second Order Incremental Feed-forward Architecture of Sigma-Delta Modulator

digital representation $\widetilde{E}(Z)$ obtained. If the digitized input signal and digitized residue is added, then the overall output can be expressed as,

$$V_{out_{ER}} = V_{SD} + \frac{2a_1a_2}{2b_1 + a_1a_2M(M-1)} V_{ref}\left(v[M-2] + .. + (M-1)v[0]\right) \tag{3.1}$$

From the Eq.3.1 it can be perceived that the inclusion of the digitized residue to the digitized input signal, brings the overall digital signal $V_{out_{ER}}$ even more close to the input signal, significantly improving the signal-to-noise ratio by the amount equal to the dynamic range of the residual ADC. Consequently, overall dynamic range can be represented as,

$$ENOB = N_{RS} + N_{SD} + 2\log_2(M) - 2 \tag{3.2}$$

where N_{RS} is the resolution of the residual ADC, N_{SD} is resolution of the ISDM and M is the OSR. With this scenario, several combinations of the resolution of the IΣΔ ADC and Residual ADC are modeled and verified in the Simulink and the optimum combination is chosen.

SIMULATION RESULTS

The ideal architecture of the IDC has been developed in Cadence environment using a second order structure with 3-bit quantizer and 5-bits ADC in the extended counting.

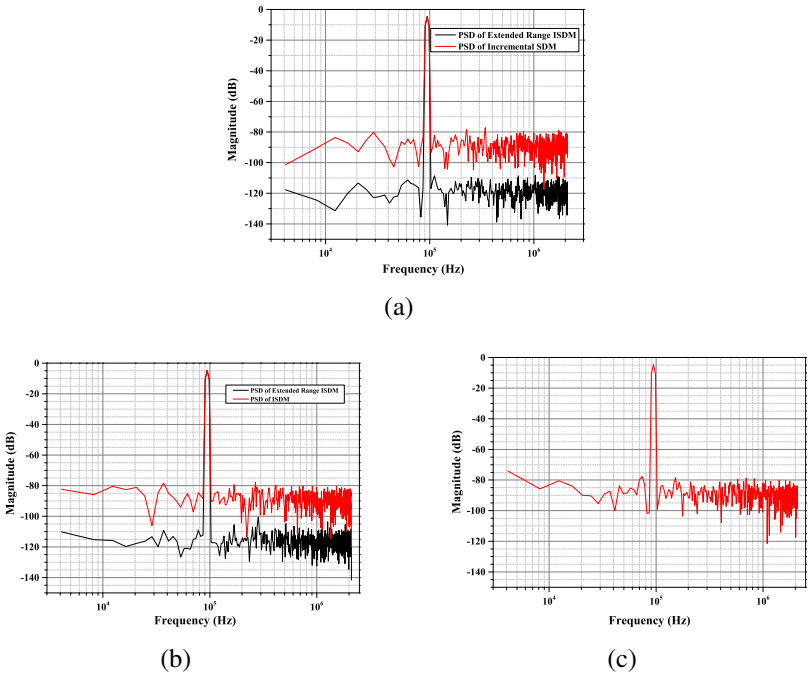

Fig. 4.1 PSD of the Extended Range Incremental SDM with (a) all the ideal blocks (b) Transistor level blocks (c) Post-layout Simulation of Incremental SDM

For second order modulator, with OSR value of 18, the expected ideal value of the SNR of the ISDM is 57 dB while that with residual ADC is 86 dB, as shown in Fig. 4.1 (a). When simulated at the schematic level, non-idealities of the blocks brings the overall SNR down to 83.7 dB (Fig. 4.1(b)). The post-layout simulation result is shown in the Fig. 4.1(c) where along with non-idealities, the parasitics also plays role, the SNDR of the ISDM, however, stays at the same level.

Acquired Credits:

- **CFU 2017/2018**
  - Scuole dott. Di Enti ricerca-Corsi (ToM) CFR 3.5
  - Partecipazione a seminari di Dottorato CRF 1.2
- **CFU 2018/2019**
  - Scuole dott. Di Enti ricerca-Corsi (ToM) CFR 8.5
  - Partecipazione a seminari di dottorato (AACD) CFR 3.6
  - Periodi di studio e ricerca allestero (Infineon) CFR 3

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