UNIVERSITÀ DEGLI STUDI DI PAVIA
CORSO DI DOTTORATO IN MICROELETTRONICA

A/D converter for serdes in 7nm FinFET technology

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Cicle: XXXIII

1. Introduction

During the academic year 2018-2019, my research, A/D converter for serdes in 7nm FinFET technology, includes four main activities. They are: the design of a voltage comparator, a capacitive DAC, a sub-channel clock generator, and a 7 bits asynchronous SAR logic.

2. Structure of the ADC

Fig. 1 shows the Asynchronous SAR ADC structure. The SAR ADC consists of digital-to-analog converters, a comparator and Asynchronous SAR logic. The SerDes system employs a 7-bit, 64-way time-interleaved SAR ADC. The ADC supports an input range of 600mV diff-pp. The ADC is simulated with a power supply voltage of 0.9V.

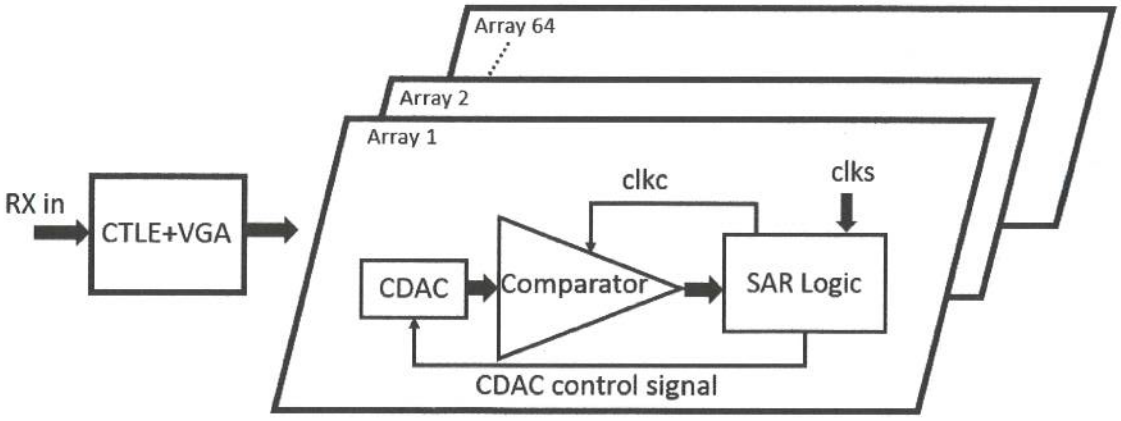

Figure 1 - Structure of the 7 bits Time-interleaved ADC

3. Comparator

The comparator is the key component for our design. It determines the accuracy, has the highest influence on speed, and contributes significantly to the power consumption. Fig. 2 shows the architecture of the strong-arm latch comparator. It consists of an n-channel input differential pair (M10-M11), two cross-coupled pairs (M1-M2, and M8-M9, respectively), and six switches, driven by the clock signal, CK. The circuit operates in two phases. When the clock signal is low, transistors M3

to M7 are turned on, keeping the two output nodes, Vout+ and Vout-, equalized and reset to the supply voltage, VDD. At the same time, transistor M12 is turned off. When CK switches to the high logic level, transistors M3 to M7 turn off, while transistor M12 enables the voltage comparison. The action of the two cross-coupled pairs is such that one output voltage goes to VDD while the other reaches ground. The main advantage of the Strong-arm latch is the high conversion speed and the zero static power consumption.

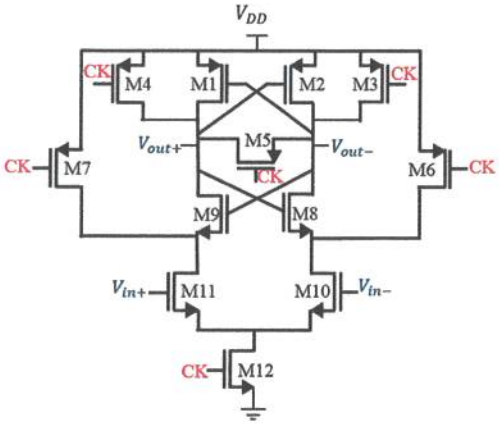

Figure 2 - Schematic of strong-arm latch

The comparator offset is an important parameter that influences the system performance. Due to the pre-charge action of M3 to M7 keeps M1, M2 and M8, M9 off initially, thereby reducing their off contribution, so the M11 and M10 are the dominant contributors. In order to analyze the offset of the comparator, a Monte Carlo simulation was carried out in the different technologies. To evaluate the offset, the input signal is varied from –15 mV to +15 in 10 ns, with an input common-mode voltage of 750 mV and a clock frequency of 1~GHz. The slope of the input signal is then 3 mV/ns. Fig. 3 shows the 200-iteration Monte Carlo histogram of the delay Td after which the comparator output switches state. Ideally, this should occur for Td = 5~ns (when the input signal is actually 0 V). The comparator offset can then be calculated in mV as Vos = 3(Td – 5), while its standard deviation σos in mV is 3σT. Fig.3 shows the result of the standard deviation is 1.90ns(5.7mV)

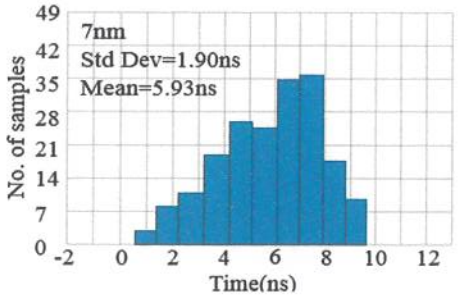

Figure 3- Monte Carlo analysis

4. Capacitive DAC

Fig. 4 shows the schematic of the capacitive DAC. The reference voltage used in CDAC is provided externally, the reference voltages are 0.9V, 0.825V, 0.7875V for VTOP, VTOP2, VTOP4, and 0.6V, 0.675V, 0.7125V for VBOT, VBOT2, VBOT4, respectively. The number for each capacitance slice is 8,4,2,1,1,1, and the last two cap arrays use the fractional reference voltage. The reason to use different reference voltage at last two slices is to reduce the total number of the unit cap and compress the CDAC

settling time. The kT/C noise limit imposes the minimum tolerable unity capacitor: 0.18 fF. this design uses the minimum value of capacitance that can be achieved in 7nm technology, 1.3fF. The CDAC control signals DAC_TOP<5:0>, DAC_CM<5:0> and DAC_BOT<5:0> are generated from the SAR logic with internal clock generator.

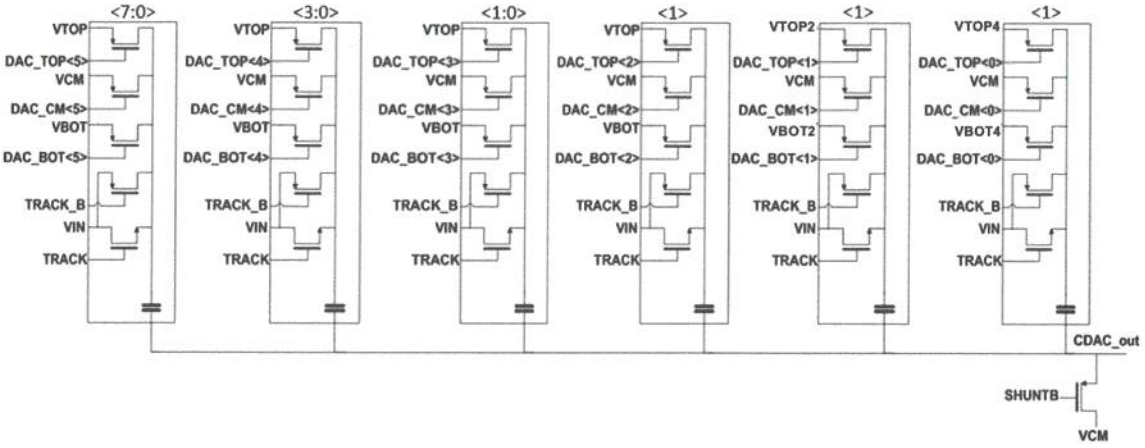

Figure 4 - Schematic of CDAC

5. Clock generator

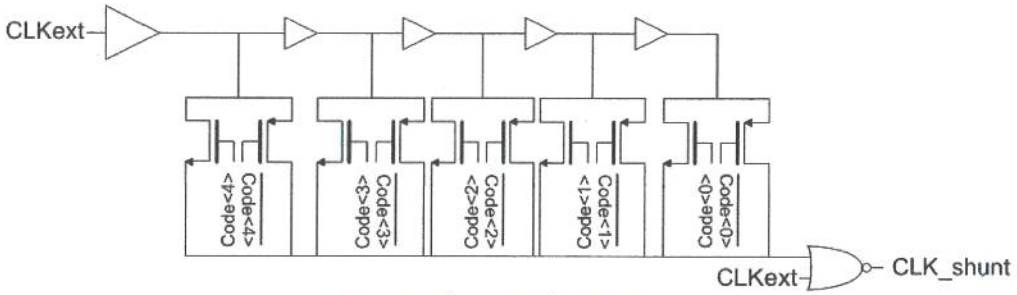

Figure 5 – Shunt signal generator.

There is only one external clock used in this design, which has a frequency of 1GHz, 50% duty cycle and 0.9V peak to peak amplitude. Fig. 5 shows the shunt signal generator. In the DAC, the designed sampling time is 38 ps, and the shunt signal generator is introduced to change the duty cycle. Fig. 6 shows the time skew block, and this block uses the shunt signal to generate the signal used in CDAC and SAR logic.

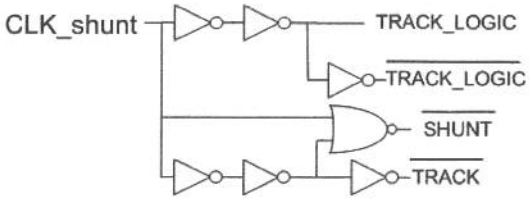

Figure 6 – Time skew block.

6. SAR logic

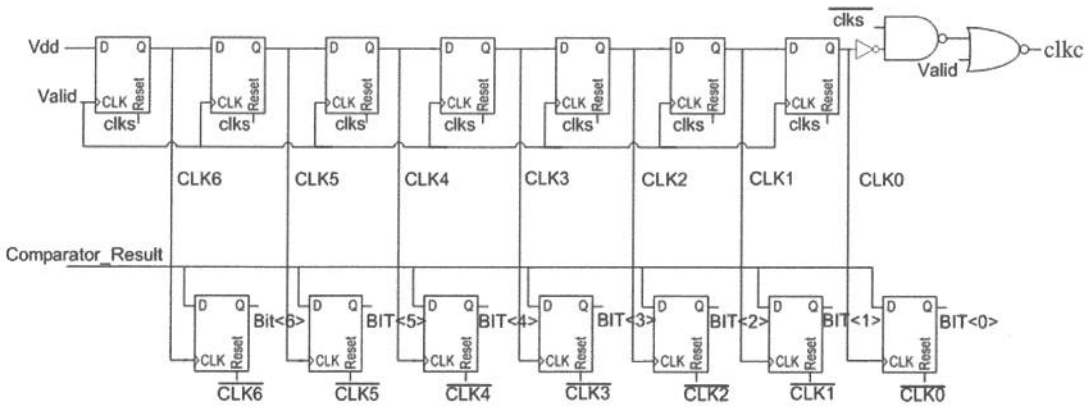

Figure 7 - SAR logic

Fig. 7 shows the SAR logic that includes two banks of D flip-flops. The cascaded D flip-flops on the top is a shift register, triggered by the comparator ready signal, and then it provides the successive step signal at CLK6 to CLK0. The time interval between the sample signal and CLK0 is the working time for the comparator, the NOR gate and NAND gate are implemented to ensure the clock of comparator reset when the last comparison finished. The bottom D flip-flops are triggered by the rising edge of the step signal, then capture the comparator output one after another, the output results of these flip-flops are sent to control the CDAC.

7. Simulation results

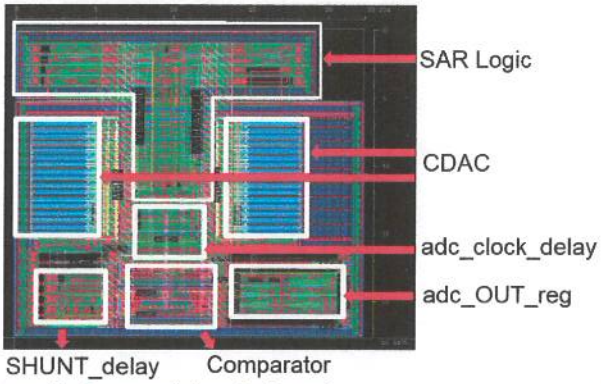

Figure 8 - Layout of the sub-channel.

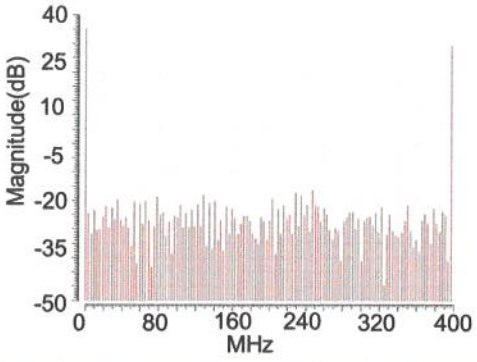

Figure 9 – FFT spectra at 800MS/s with 399-MHz input

Fig. 8 shows the layout of the sub-channel. Due to a problem of missing code, verified in PLS simulations, an extra delay is added to the clock of the comparator. The reported PLS results are with the extraction of each internal block without the layout of internal blocks connections. The core sub-ADC occupies an active area of 22.65 μm × 22.22 μm, as shown in Fig. 8. The maximum sampling rate is 800MS/s. Fig. 9 shows the achieved FFT spectrum: the SNDR is 38.2 dB and the corresponding ENOB is 6.05 bits.

Zhaochen Yin

Prof. Edoardo Bonizzoni

Università di Pavia

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ATTIVITA' PREVISTE NELL'ANNO ACCADEMICO (con certificazione)	ore o num	CFU
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1b,c) **Scuole di Dottorato, di Enti di Ricerca, Corsi intensivi** (0.2 CFR / ora) .....IOT..... ... .ADCC 2019.....	/	8.93
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Il dottorando Zhaochen Yin **Visto del tutore:** E Bonizzoni

Piano approvato / modificato il 9../23/.....2019 **Il Coordinatore:** _____