Developing a Way of Self-Interference Cancellation

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Introduction

The large difference between the maximum TX power and the minimum required RX sensitivity demands a method to attenuate the signal power of the strong TX self-interference (SI) signal, which is particularly true in high-performance applications such as Wi-Fi, and evolving fifth generation (5G) wireless standards. An ideal self-interference cancellation (SIC) should contribute minimal noise to the RX front end, occupies minimal silicon area, and has minimal added power consumption. There have been numerous recent efforts to perform on-chip SI cancellation in the analog/RF front end.

Assume that an FDD wireless system with $P_{TX,main}$ = +20 dBm, 60 MHz RX BW, and 8dB RX NF (NF_{RX}), SIC of 20dBm-(-174dBm/Hz+8dB+78dBHz)+4dB~110dB is required (which is shown in Fig. 1 below). Duplxer could attenuate +40 dB of TX power, therefore, it is necessary to reach SNR close to +70db with the cancellation design. Additional 4 dB cancellation has been assumed to ensure that the residual SI is well below the RX noise floor. Such a large amount of isolation/cancellation must be achieved by combining suppression at the antenna, analog and digital domains [1].

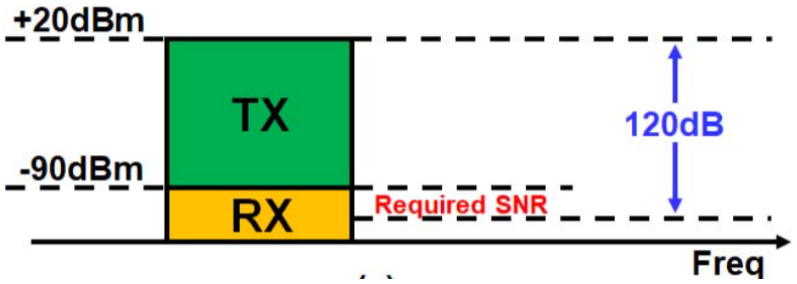

Fig.1 SI cancellation requirement

The proposed cancellation method is shown in Fig. 2 (the components are selected by red starts are developed by me), and the actual design are fully differential. In our method, cancellation happens in the boundary of RF and Base-Band (BB). Hence, it does not needs high RF power for cancellation and caused nonlinearity in the RF parts. It does not also lead to nonlinearity in BB.

Capacitive DAC (CDAC)

Capacitive DAC (CDAC) has some advantages and disadvantages which is mentions in the first year report. It is important to just mention that it is less sensitive to clock jitter since it should just deliver the whole charge in contrast to current DAC. However, it can creates a lot of high frequency harmonics [3].

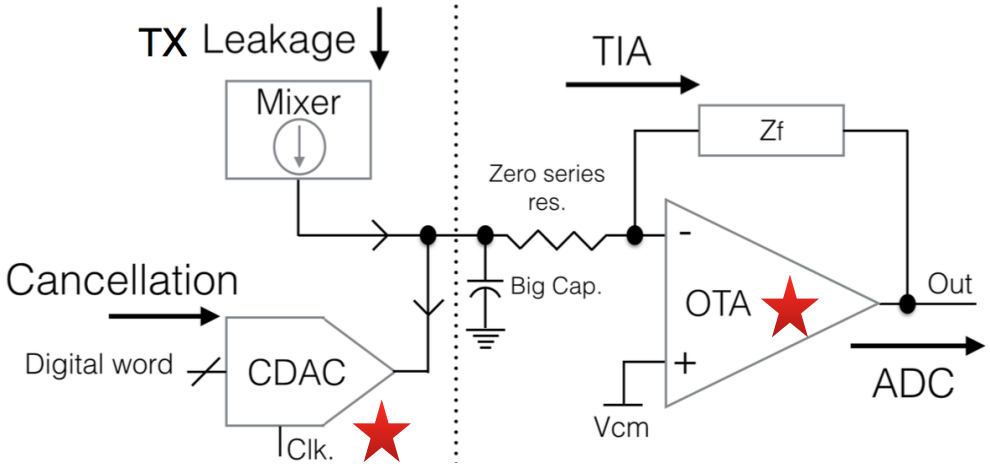

Fig. 2 Schematic of cancellation system

According to calculations in the first year report, for the specific amount of cancellation, the total capacitance and number of bit is almost should be equal 1pF and 10-bits, respectively. The CDAC with split-capacitor was chosen as CDAC that is shown in Fig. 3 (original one is fully differential). It includes 3-bits (binary weighted) LSB, 2-bits (binary weighted), and 5-bits (thermometric cells). By using thermometric way in the last bits (5-bits MSB), the linearity of system is improved.

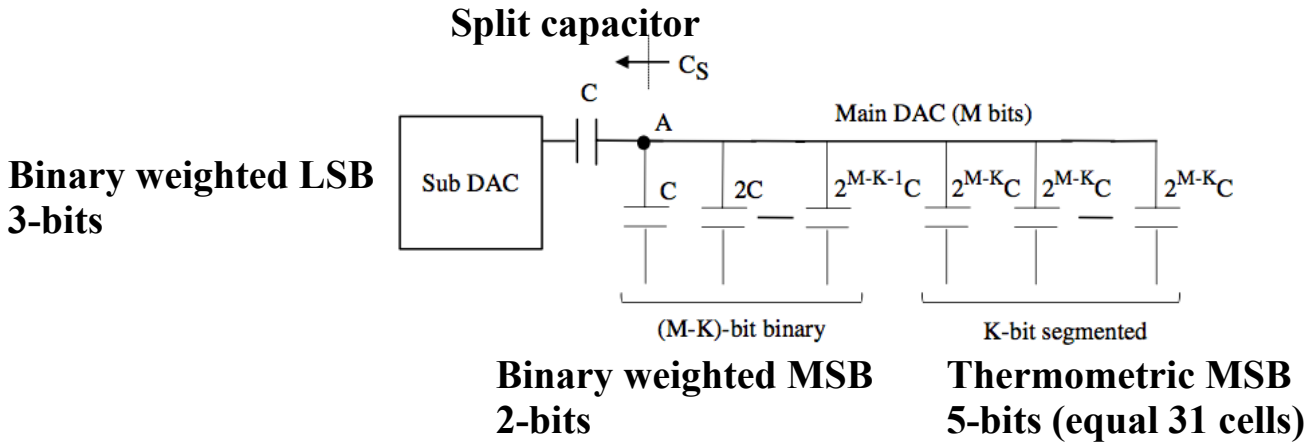

Fig. 3 Configuration of the CDAC

The CDAC has Vref+ and Vref- equal 0.35V and -0.35V, respectively. Split-capacitor CDAC has two important problem as follows: unequal parasitic capacitance to ground from each node of attenuator capacitor and attenuator capacitor is non-integer amount of unit capacitance. The former is fixed by using the MOM capacitor which has the same parasitics on two nodes of MOM capacitor as it is shown in Fig. 4. The latter is dealt with by solution is presented in [2]. By adding the extra capacitor (CX) on LSB side shown with in Fig. 5, the attenuator (CBX) could be integer multiplying of the unit capacitor.

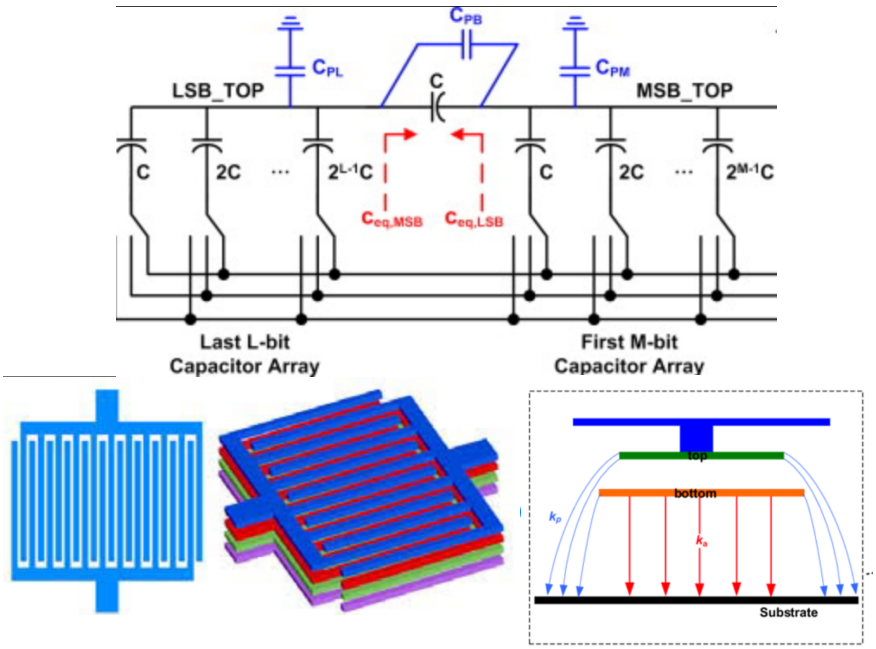

Fig. 4 MOM capacitance and CDAC with split-capacitor configuration

Non-fractional

L	C_X	$C_{BX} = \left(\frac{2^L}{2^L-1} + \frac{C_X}{2^L-1}\right)C$
4	14	2C
5	30	2C
6	62	2C
$V_{L+/-}$ stays within supply rails		

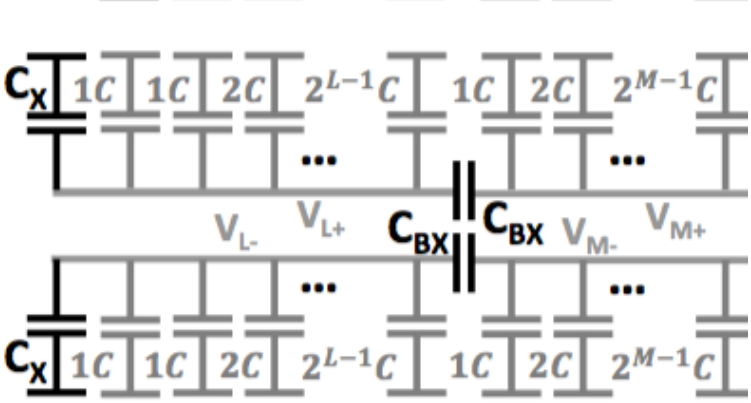

Fig. 5 MOM capacitance and CDAC with split-capacitor configuration

Unit capacitance of the CDAC should be chosen in order to meet criteria of noise and matching. 8fF capacitance is chosen to provide the capacitance equal 1pF. Its standard deviation is 18aF which is acceptable. Total power of noise of the CDAC almost equal (2*KT/$C_{total\ MSB}$) which is acceptable.

Special consideration should be taken into account Over drawing the layout of the CDAC. It should be drawn in matrix shape in order to improve the linearity of the CADC and overcome the systematic and random errors. *For measuring linearity and parasitics of the CDAC layout of the CDAC is drawn shown in Fig. 6.* Each cell is compromised of four unit capacitors with some local control logic in order to decrease noise and energy. However, in some cells either less unit capacitors or no unit capacitor are used.

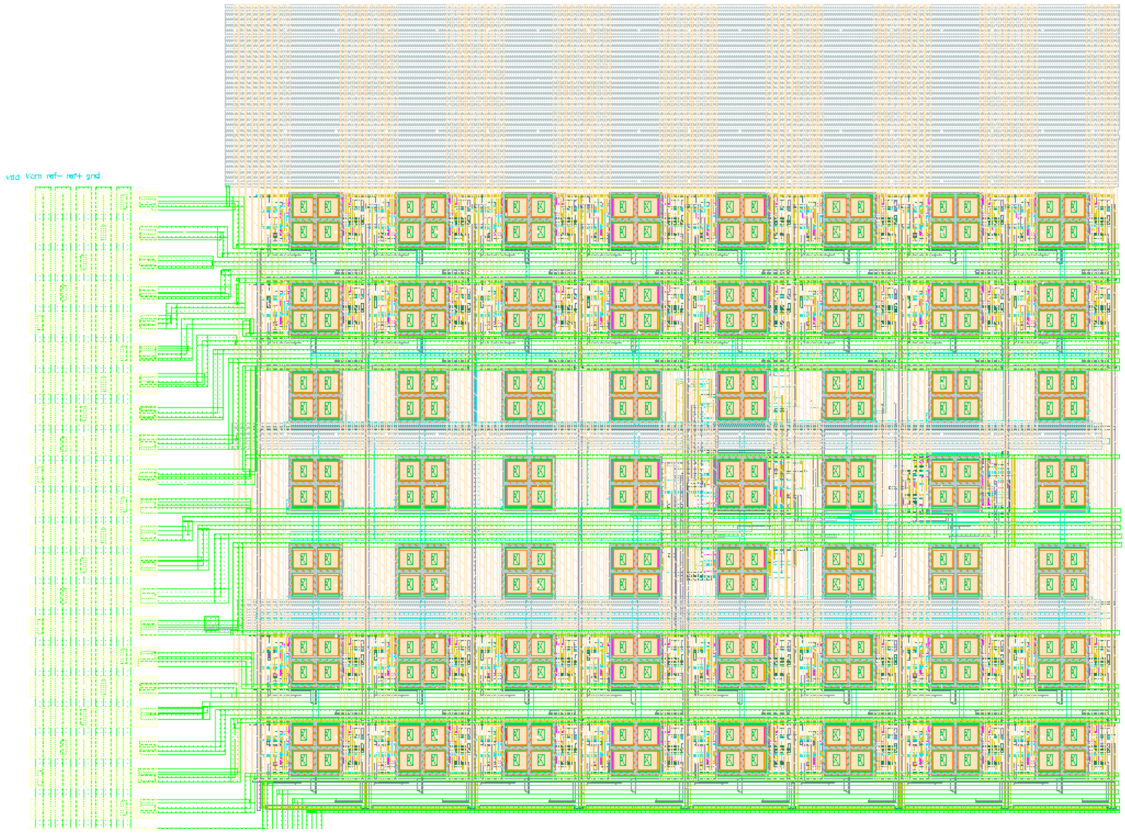

Fig. 6 Drawn CDAC physical layout

Switches of CDAC

In order to have the less parasitics, low voltage MOS was used for developing the switch, however, it limits amount of the swing of the CDAC which is corresponding to amount of cancellation. LSBs' and MSBs' switches are chosen with non parasitic insensitive and parasitic insensitive switches, respectively.

CDAC Calibration

The 5-bit thermometric MSB array will be self-calibrated, foreground Calibration.

The 5-bit LSB array is composed of the Left and right side of attenuator capacitor are not calibrated.

The calibration circuitry includes

- A slow-speed high precision 12-bit calibration analog-to-digital converter (CALADC)
- A small 6-bit (low resolution for better calibration) binary-weighted capacitive calibration DAC (CALDAC)
- A 63-word 6-bit-per-word SRAM, a bias generator
- Some control logic blocks.

First order filter (TIA)

First order filter or TIA has main role in the receivers and our design. It filter out unwanted signal and provide the virtual ground (low impedance node) in the output of mixer. Also, in our design, it provides virtual ground for the CDAC.

Our TIA should have some vital specifications:

- Working on low voltage in order to increase the amount of cancellation.*
- Having special gain (in doublet frequency) in order to compress pole-zero (doublet frequency) and lower settling time of the CDAC.**
- Ability to follow system speed
- Acceptable power consumption

* DAC references are limited from one hand to maximum working voltage of the switch (1V for low voltage switch) and from another hand, it should have symmetry around common mode voltage of TIA. If the TIA work with 1.3V, its common mode voltage is 0.65. Hence one of the references is 1V and another one is [0.65 -(1-0.65)= 0.3]. It is somehow hard to design TIA with high gain with 1.3V supply voltage. So, we could not decrease the Supply voltage less than 1.3V. Most of the designed TIA like our configuration works with a voltage supply more than 1.5V.

* * Frequency of doublet comes from the feedback and it is around 60MHz. For decreasing the effect of pole-zero the loop gain at the doublet frequency should be more the certain level. If we consider feedback resistor and capacitor and impedance at the input of the TIA, this gain should be more than 50dB for reaching to 0.1% (which equal 10-bits DAC) accuracy without any negative effect comes from doublet.

As you can see in Fig. 7, the TIA is three stages. It is composed of there stages to obtain high gain. First stages is folded cascade because it should work with the low voltage.

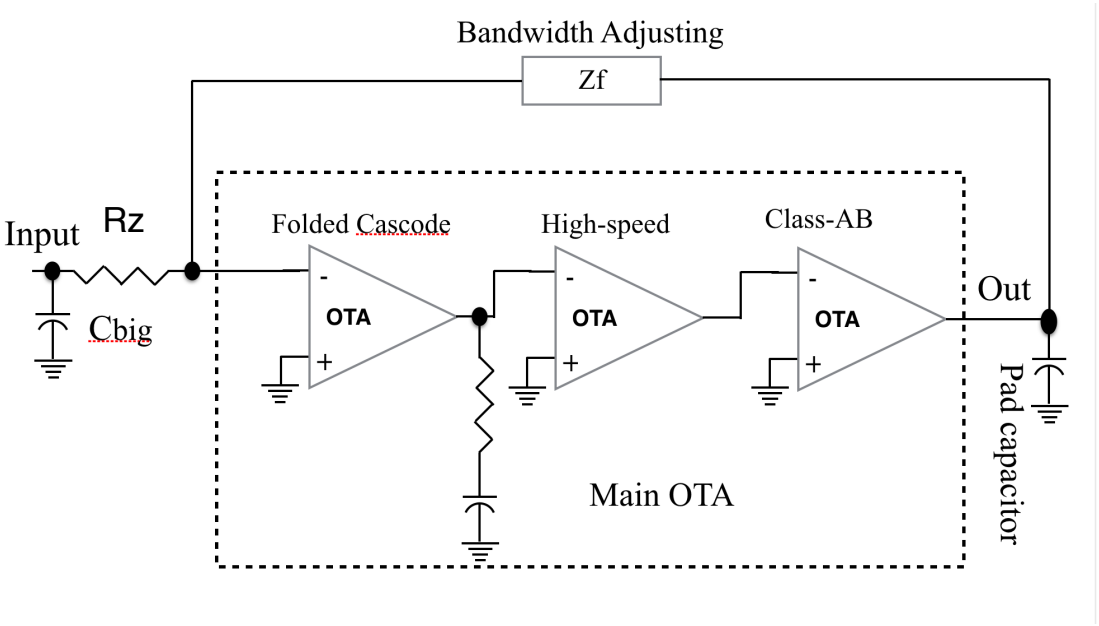

Fig. 7 Developed TIA Building Block

There is zero at the output of the first stage for extending the band-width. At the input of TIA, there is Rz and Cbig could create high-frequency of zero for improving the phase margin. Capacitance of Cbig cannot be small because it should shunt the high frequency components come from mixer. It could not also be so big since it amplifies the noise at the output of the TIA. The summary of the designed TIA is reported in table below.

A working frequency of the DAC is chosen 800MHz, so TIA should settle within 640ps. “f” is feedback factor , hence, f*Wu is equal to time constant (tau) of the system.

f= Cf/(Cf+Cbig) and 6* Tau ~640>> around 2.5GHz

By considering the pole-and zero of the system and gain at doublet , the amount of DC gain should be more than 80dB.

Simulation result of the designed TIA

Working Voltage	Current counsumption	Unit-Gain-Frequncy	DC gain	Phase Margin
1.3V	4.3mA	2.7GHz	82dB	46’

G-loop of this TIA is shown below.

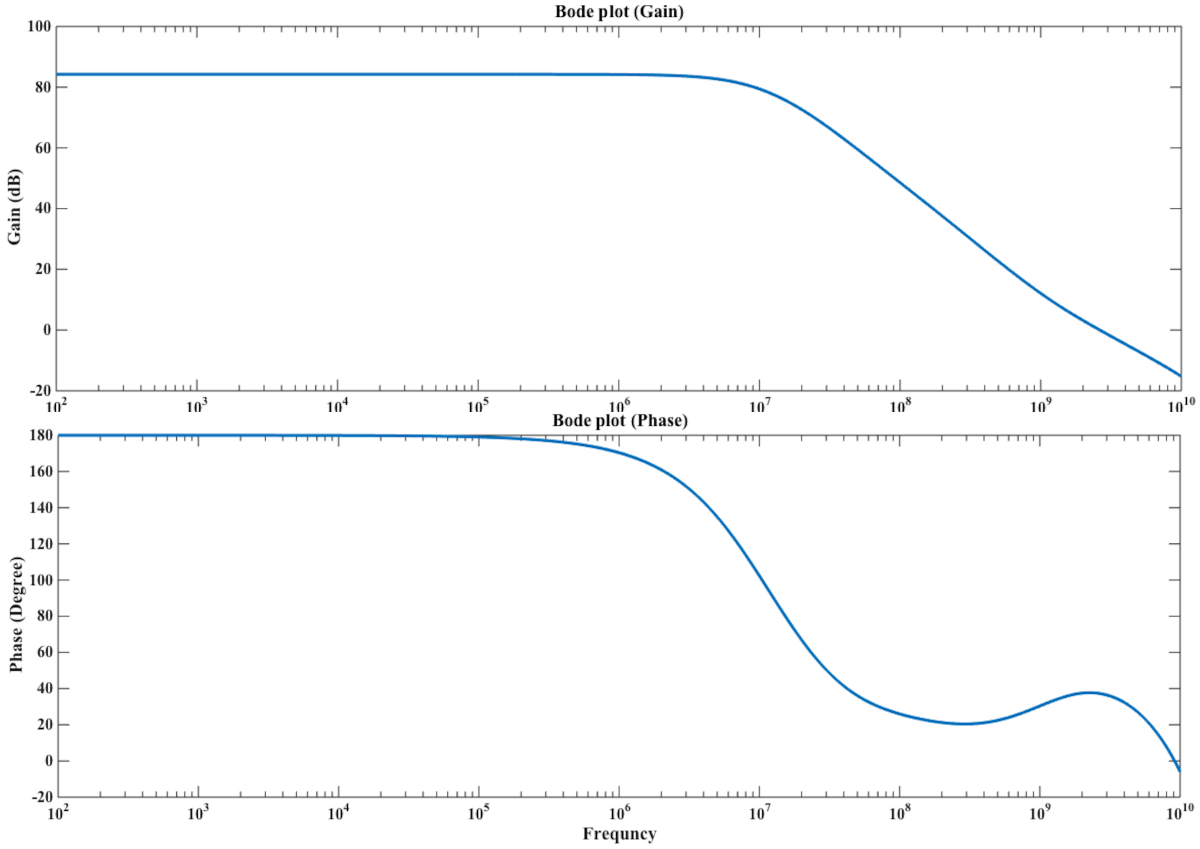

Fig. 8 TIA G-loop

For a view about settling time of the system, a test bench is prepared and put some components equivalent to the CDAC circuit as shown in Fig. 9. The result with the designed TIA is shown in Fig. 10. The high gain of the TIA compress the doublet and system could settle to 0.1% over 575ps. So the speed, gain , and pole-zero configuration the TIA could be useful for our design.

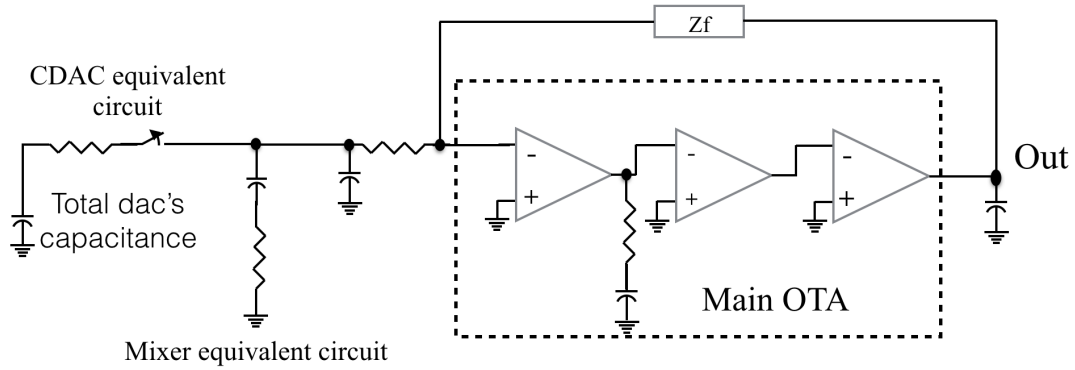

Fig. 9 Settling time test-bench

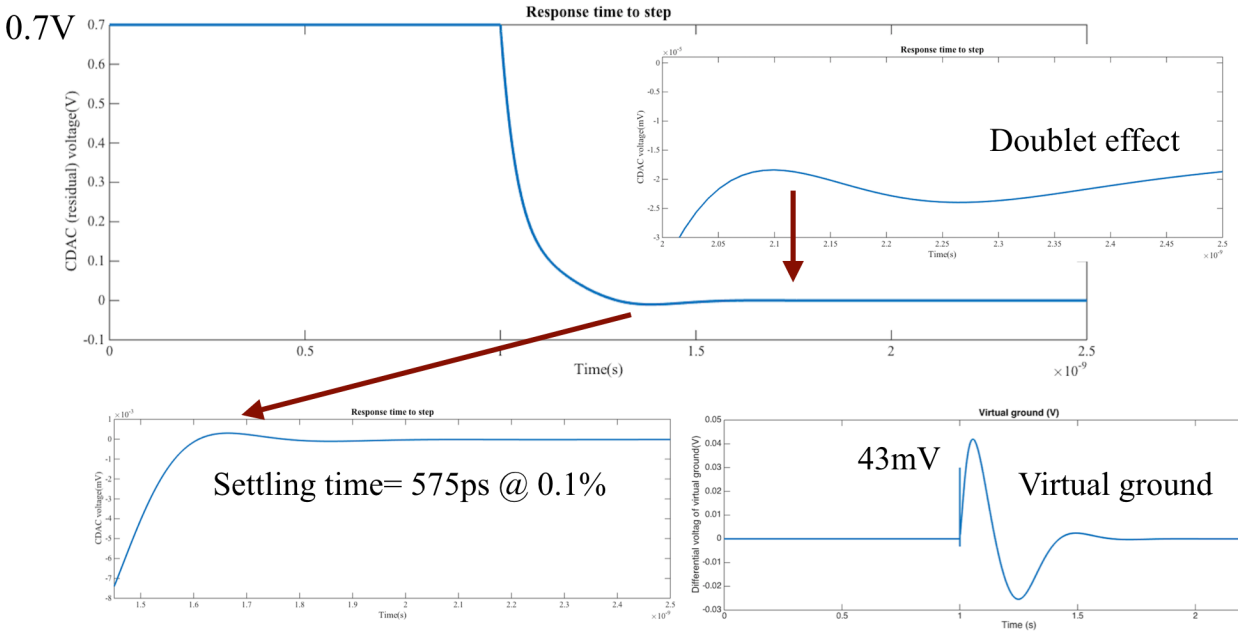

Fig. 10 Settling time graph

Cancellation Test

The cancellation is tested according to configuration in Fig. 2 (in fully differential application). Some important parameter is as follows:

- 10-bit differential time-interleaved CDAC

- Total capacitance in each side is equal 1pF
- CDAC voltage reference equal to +/-0.35V
- DAC and LNA clock frequency 800MHz/ RF signal frequency 820MHz
- Maximum output signal of CDAC
- All the circuits are comprised of real and designed blocks expect clocks and mixer
- Mixer works in 50% duty cycle

Spectrum of signal is shown below in Fig. 11, The amount of cancelled (in dBc) represented with positive numbers. For example, magnitude of competent of 20MHz is +60dBc means which means the 20MHz signal -60MHz is cancelled related to original signal.

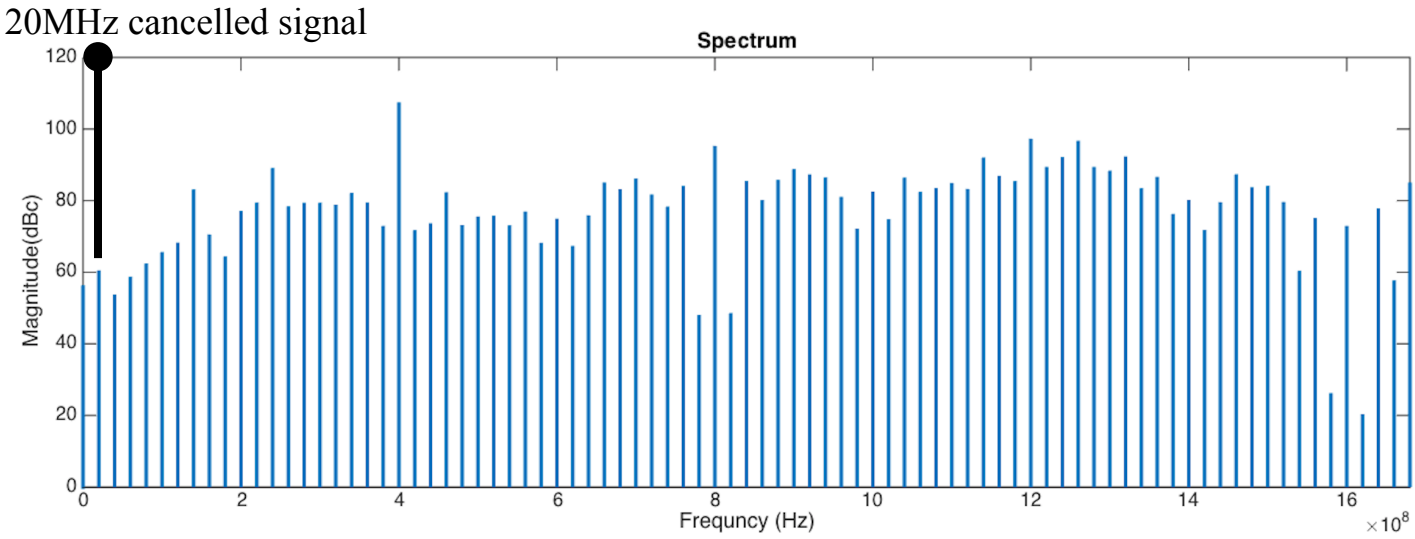

Fig. 11 Spectrum of the signal after cancellation (Represented by positive number)

[1] T. Zhang et al. "Wideband Dual-Injection Path Self-Interference Cancellation Architecture for Full-Duplex Transceivers" JSSC, 2018.

[2] A. H- Chang et al. "A 12b 50MS/s 2.1mW SAR ADC with Redundancy and Digital Background Calibration" ESSCIRC, 2013.

[3] Nandi, S. Pavan "A Continuous-time ΔΣ Modulator with 87 dB Dynamic Range in a 2 MHz Signal Bandwidth Using a Switched-Capacitor Return-to-Zero DAC" CICC, 2012.