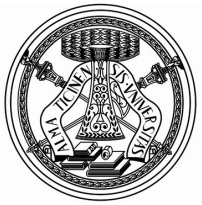

UNIVERSITA' DI PAVIA

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CORSO DI DOTTORATO IN MICROELETTRONICA

Single-stage Two-steps Extended-Range Second-order Incremental ΣΔ ADC Design

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Annual Project Report 2019-2020

INTRODUCTION

Analog-to-Digital converters (ADCs) used in automotive applications often require very high absolute accuracy and linearity, as well as very low offset and noise with low power consumption. The properties of incremental A/D converters (IADCs) are well matched to the automotive requirements. They provide very precise conversion with accurate gain, high linearity, and low offset, and the conversion time can be relatively short. The key property of these converters is that they do not rely on precisely matched analog elements to achieve high resolution, but on oversampling, noise-shaping, and digital post-filtering. Thus, these converters can be integrated well into today's fine line-width CMOS technologies. The ADC proposed is targeted to achieve an effective number of bits (ENOB) equal to 12 at a clock frequency of 80 MHz, with a conversion time lower than 25 clock cycles.

INCREMENTAL ADC

The SAR ADC approach has limitations meeting these requirements. Hence, the alternative is to contemplate about a hybrid architecture. Since, the specified requirements are in line with the characteristic of the IADC, thus a productive alternative.

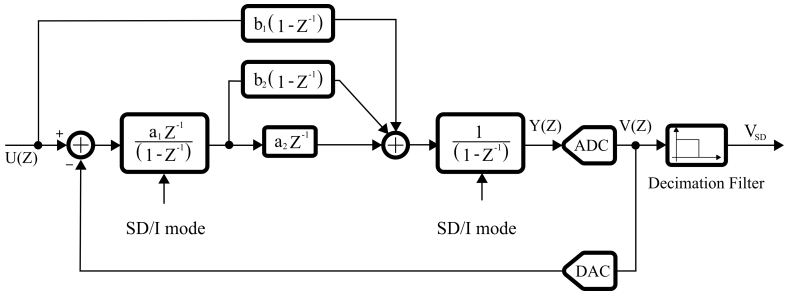

Fig. 2.1 Second Order Incremental Modified Feed-forward Architecture of Sigma-Delta Modulator

The block diagram of IADC shown in Fig. 2.1 consists of two integrators followed by a multi-bit quantizer and a feedback DAC. In order to reuse the same hardware to digitize more than one analog input signals, reset feature is incorporated in $\Sigma\Delta$ modulator, hence the name Incremental Sigma-Delta Modulator. The structure is reset at the beginning of the new conversion cycle including analog and digital memory elements. Then sample is acquired using sample and hold circuit and is applied to the structure for conversion. Provided that the oversampling ratio M is high enough, the reconstruction can be achieved by passing the output signal through a decimation filter with down sampling by a factor of M i.e. OSR. Thus output can be represented as in Eq 2.1.

$$V_{SD} = \frac{2}{M(M-1)} V_{ref} \left(v[M-2] + ... + (M-1)v[0]\right) \tag{2.1}$$

Where V_{SD} represents the digital equivalent of the input sample.

The obtainable effective number of bits (ENOB) can be expressed as,

$$ENOB = N_{SD} + 2\log_2(M) - 2 \tag{2.2}$$

where, N_{SD} is the resolution of the quantizer used in $\Sigma\Delta$ loop and M is the OSR.

PROPOSED ARCHITECTURES OF ERADC

The resolution of an IADC can be improved over that obtained with the simple decimation described above in Eq. 2.2 by using an estimate of the residual error V_{RS} to reduce the quantization noise at the output of the modulator where the residue of the modulation is the difference of output of the second integrator, output of first integrator and the input. Shown in Fig. 3.1 is the conventional block diagram of the ERADC where separate ADC hardware (RADC) is employed for the residue evaluation. Fig. 3.2 shows the proposed architecture. Here, the same hardware of Incremental ADC is reused for coarse as well as fine quantization.

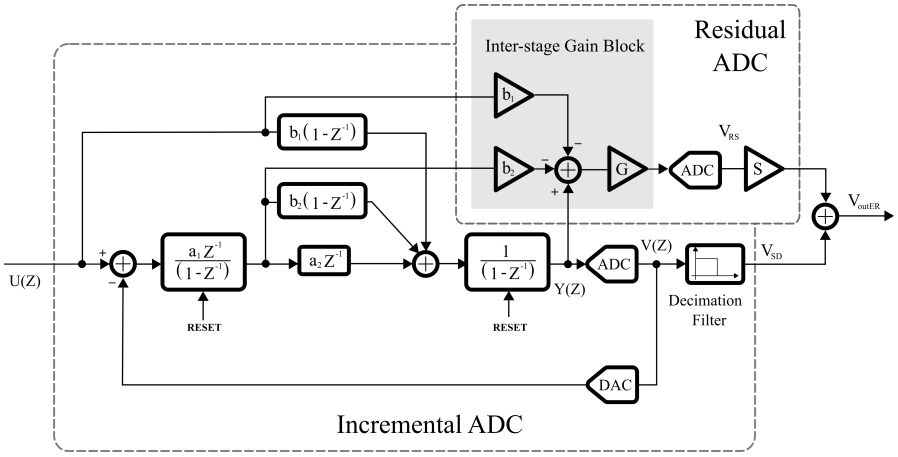

Fig. 3.1 Conventional Architecture of ERADC

In the coarse quantization phase, the switch with control signal Φ_{input} is closed and that with $\Phi_{residue}$ is kept open and IADC structure is iterated over M_1 clock cycles i.e. OSR for coarse conversion. The coarse output is then saved in the memory element. In the last clock cycles, Inter-stage Gain block calculates the residue. Further, the residue evaluated is fed to the same IADC hardware reusing it even for residue digitization by closing the switch with control signal $\Phi_{residue}$ and opening the one with control signal Φ_{input}. IADC is iterated, then, over M_2 clock cycles i.e. OSR for the fine quantization and digitized residue output is obtained. Ultimately, the two outputs are recombined with proper coefficients, can be expressed as,

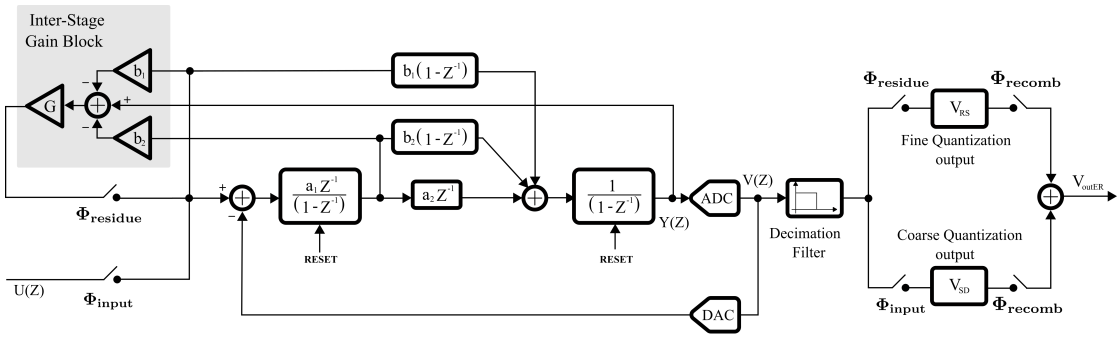

Fig. 3.2 Proposed Architecture of ERADC

$$\begin{aligned} V_{out_{ER}} &= \frac{2}{M_1(M_1-1)} V_{ref}\left(v[M_1-2]+..+(M_1-1)v[0]\right) \\ &+ \frac{2}{M_2(M_2-1)} V_{ref}\left(v[M_2-2]+..+(M_2-1)v[0]\right) \end{aligned} \tag{3.1}$$

From the Eq.3.1 it can be perceived that the inclusion of the digitized residue to the digitized input signal, brings the overall digital signal $V_{out_{ER}}$ even more close to the input signal, significantly improving the signal-to-noise ratio by the amount equal to the dynamic range of the residual ADC. Consequently, overall dynamic range can be represented as,

$$ENOB = 2N_{SD} + 2\log_2(M_1) + 2\log_2(M_2) - 4 \tag{3.2}$$

where $N_{SD} = 3$ is resolution of the IADC. The OSRs chosen are $M_1 = 18$ and $M_2 = 5$. With this combination of the parameters, the ENOB obtained from coarse quantization is 9-bits while overall with fine quantization, it achieves 14-bits.

SIMULATION RESULTS

The architecture of the IADC has been developed in Cadence environment using a second order structure with 3-bit quantizer and OSRs $M_1 = 18$, $M_2 = 5$. The SNDR obtained with coarse and fine quantization in ideal simulations 60 dB and 86 dB, at transistor level those are 60 dB and 70 dB while in extracted simulations those are 60 dB and 73 dB respectively. Characterization of the first chip has been done which involves the measurements of only oversampling ADC which can be configured into Sigma-Delta (SD) mode and Incremental (I) mode. The SNR and SNDR attained, When configured in SD-mode is 66 dB and 63 dB and when configured in I-mode is 59 dB and 55 dB respectively.

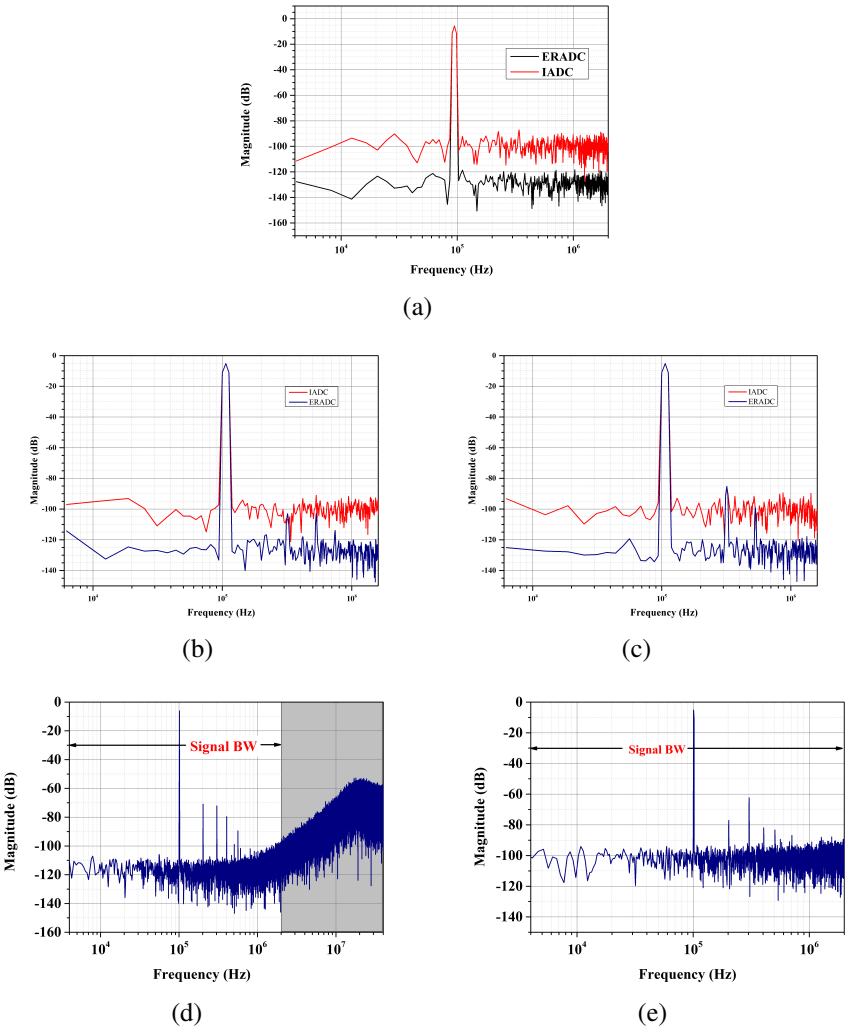

Fig. 4.1 PSD of the Extended Range Incremental SDM with (a) all the ideal blocks (b) Transistor level blocks (c) Extracted Simulations (d) Measured PSD in SD-mode (e) Measured PSD in I-mode

Acquired Credits:

- **CFU 2017/2018**
  - Scuole dott. Di Enti ricerca-Corsi (ToM) CFR 3.5
  - Partecipazione a seminari di Dottorato CRF 1.2
- **CFU 2018/2019**
  - Scuole dott. Di Enti ricerca-Corsi (ToM) CFR 8.5
  - Partecipazione a seminari di dottorato (AACD) CFR 3.6
  - Periodi di studio e ricerca all'estero (Infineon) CFR 3
- **CFU 2019/2020**

- Insegnamenti ufficiali UniPV o corsi graduate (AIC) CFR 9
- Presentazione di lavori a congressi internazionali CFR 2
- Titolarità di seminari specialistici di ricerca CFR 2.4

- **CFU 2017-2020** **CFR 33.5**

Publications:

- A. Taralkar, F. Conzatti, P. Malcovati and A. Baschirotto, "Analysis of Operational Amplifier Requirements for Extended-Range Second-Order Incremental ADCs," 2020 *27th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* 2020, pp. 1-4, doi: 10.1109/ICECS49266.2020.9294870.
- A. Taralkar, F. Conzatti, P. Malcovati and A. Baschirotto, "A Dual-Mode Second-Order Oversampling Analog-to-Digital Converter", *Accepted in ESSCIRC 2021*

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