The third-year report

Topic: Proposing a self-interference cancellation technique (for wireless communication applications) with a capacitive DAC.

I would like to explain the last year achievements (about my thesis) here. The report is composed of the four different parts as follows.

1- Shortly explanting about the application.
2- Elaborating on the sub-blocks.
3- Explaining the design points along with reporting the simulation results.
4- Showing the final layout
5- References

1- Self-interference cancellation (SIC)

The goal of my project is to be developed a mixed-signal design embedded in the full-duplex or frequency-division duplexing receivers to remove the residual transmitter signal (Self-interference signal) in the receiver path. It relaxes the specifications of the following blocks including dynamic range of the ADC. The right-side of fig.1 has been developed in my thesis, and the design specifications and basic parameters of my project is defined in ref. [1], one of our group prior project.

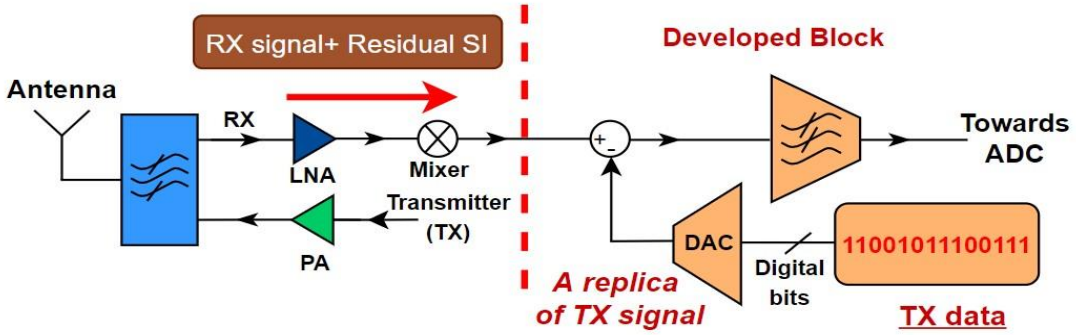

Fig. 1 The system-level block diagram including RX and SI signal.

The developed circuits could be simulated and worked in the two different modes:

A. As a stand-alone capacitive DAC (CDAC).
B. Or SIC block.

2- Sub-blocks

Four main sub-blocks are designed in 28-nm CMOS technology, and they are shown in fig. 2. The sub-blocks are categorized as follows:

I. First order filter or TIA
II. C-array
III. The built-in self-test circuits and digital controller section
IV. Output buffer

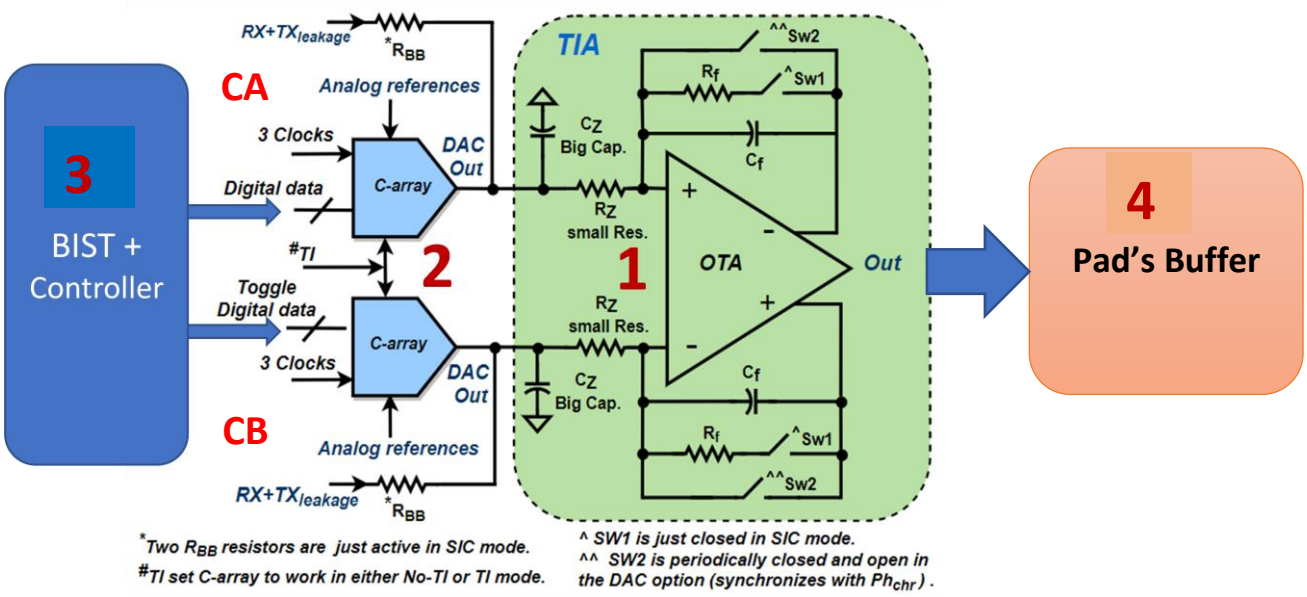

Fig. 2 Developed sub-blocks for SIC application.

2-1) TIA

The TIA's duties are to

1- remove the high frequency components in the RX chain because of the RF signal or the C-array switching.
2- amplify the RX's weak signal.
3- provide and necessary current for either charging or discharging the c-array.
4- put almost a constant voltage at the outputs of the C-array by virtual ground.

The TIA of is composed of the three main parts as shown inside of the green area in fig. 2, as mentioned below:

- Input R_Z/ C_Z : Filtering the spikes at the input of the TIA and creating a zero in the open-loop transfer function of the TIA.
- Feedback R_f/ C_f: Adjusting the receiver bandwidth and part of amplification gain for the receiver's weak signal.
- The OTA consists of the four sub-blocks, as shown in the fig. 3 below.

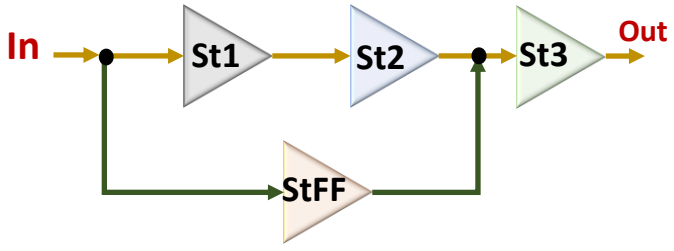

Fig. 3 The OTA structure.

2-2) C-array

- The C-array resolution was calculated to be equal to 10-bit and could works in the time-interleaved (TI) in SIC mode to increases cancellation's frequency.
- Since the number of bits of the C-array is relatively high to be built in the fully binary way, the split-capacitor technique could be a good candidate for implementing the C-array. For fixing the critical issue of the split-capacitive DAC (fractional value of the split capacitor), a special technique (introduced in ref [2]) has been used.
- We also use segmentation technique to improve the linearity of the CDAC [3].

The C-array divides up three parts as its *single ended model* is shown in fig. 4.

- *3-bit binary cell: first three LSB (in the left-side)*
- *2-bit Binary cell: the next two bits (in the middle)*
- *5-bit thermometric cell: the five most-significant bits (in the right-side).*
- *The used capacitance are as follows $1*C_U$, $2*C_U$, and $4*C_U$ in this design.* Hence, it has positive effect on the linearity of the CDAC.

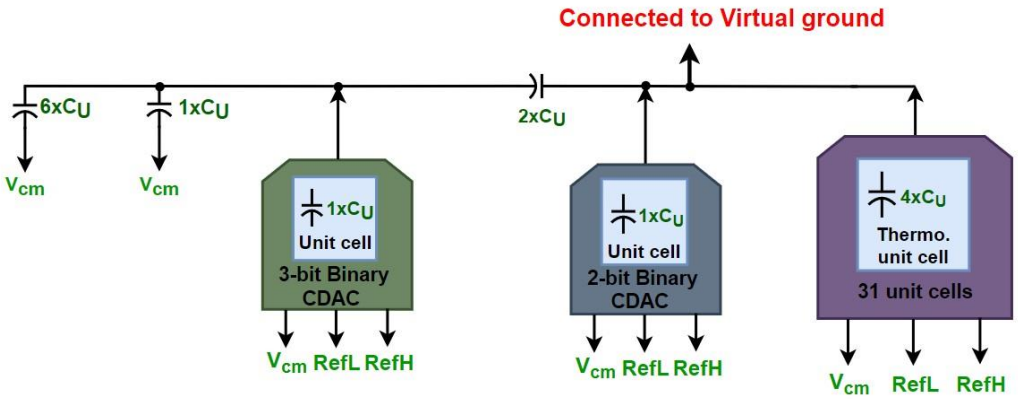

Fig. 4 Single-ended model of the C-array configuration.

2-3) Digital section

This part has two main duties.

- Built-in self-test (BIST): It is created by *Verilog (HDL)* and generates the necessary data for properly testing of block in each working mode (a digitized sinusoidal waveform with the different amplitude and frequency). It receives serial data from the outside of the chip to determine its working mode.
- Clock generator: It controls the clock and working-mode of the block in the CDAC or SIC modes. It also provides the main high-frequency clock of the chip.

2-4) Output buffer

The pad and probe capacitance (in total around 1pF) negatively affects the performance of the TIA, so it is vital to have a buffer between the output of the TIA and the outside of the chip. The capacitance of two different capacitors to the ground equal:

- Pad capacitance: it is more than 500fF in our technology.
- Probe capacitance: 300fF could be a good approximation for our device.

3- Simulation results

The circuits are designed and simulated in 28-nm CMOS technology. It could be simulated in four different modes as it shown in the table I (Each C-array works with clock frequency of 1GHz) – the fig.5 could help better explain the working modes:

Table I the working mode of the designed block.

Mode	Sub-blocks	Description	Application
1	TIA	C-arrays are off	Characterizing the TIA
2	1 C-array + TIA	One of the C-array works	Characterizing CDAC-A or CDAC-B
3	2 C-array + TIA	Two of C-array works together with the same clock	Two-tome test of two CDAC
4	2 C-array + TIA	Two of C-array works in the time-interleaved mode	Self-interference cancellation

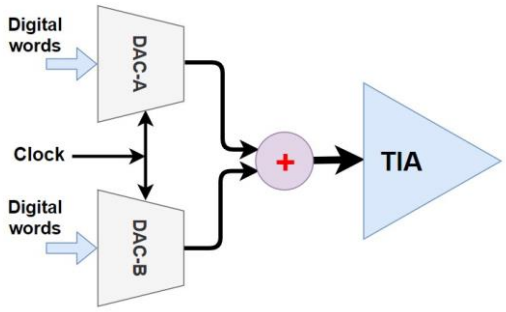

Fig. 5 DAC modes

The complete details of the design are available on my 1st and 2nd year reports.

3-1) TIA's characteristics

The TIA should fulfill some important specification as follows.

- Lowering the settling time of C-array.
- Improving the accuracy (performance) of the analog signal (output of the TIA).

There are various design criteria to fulfill the mentioned specifications. A few of them are explaining below.

1) Open loop gain of TIA should be high enough to decreases the negative effect of the pole/zero doublet on the settling time of the C-array. The one of pole and zero pair is caused by feedback and input networks.
2) The dominant poles and zeros (in the open loop response of the TIA) should be arranged to get enough unity-gain bandwidth and phase-margin. We used here two-pole/one zero compensation method (high-frequency zero).
3) The input referred noise is also important design's parameter.

The table II and fig. 5 show the short specification of the TIA and the power consumption of different stage, respectively. The break-down chart indicates the complete power consumption of each stage including the bias and CMFB of each one.

Table II the brief specifications of the TIA.

V_{ddA}	Power consumption (mW)	Input referred noise (V_{rms})	Open-loop Spec. (G-loop)	Unity-gain-bandwidth (GHz)	Phase Margin (Deg.)
1.3	9.2	85		4.6	53°

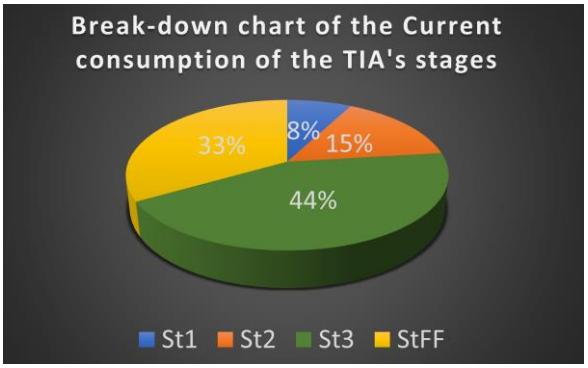

Fig. 6 Break-down of power consumption of TIA's stage.

The test-bench and frequency response of open loop of the TIA is shown in fig. 7 and fig.8, respectively. The left side of the fig.7 selected with the orange color model the equivalent C-array in this test, and the red symbol shows where the probe is located.

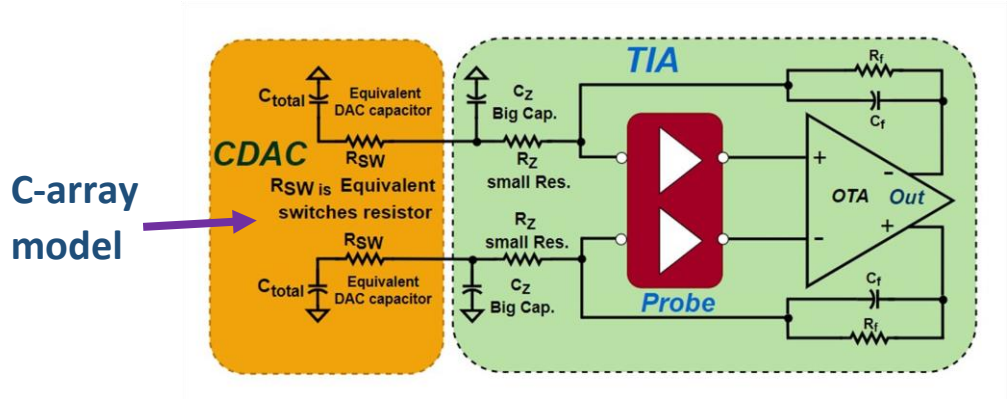

Fig. 7 Test-bench for measuring the open loop characteristics of the TIA.

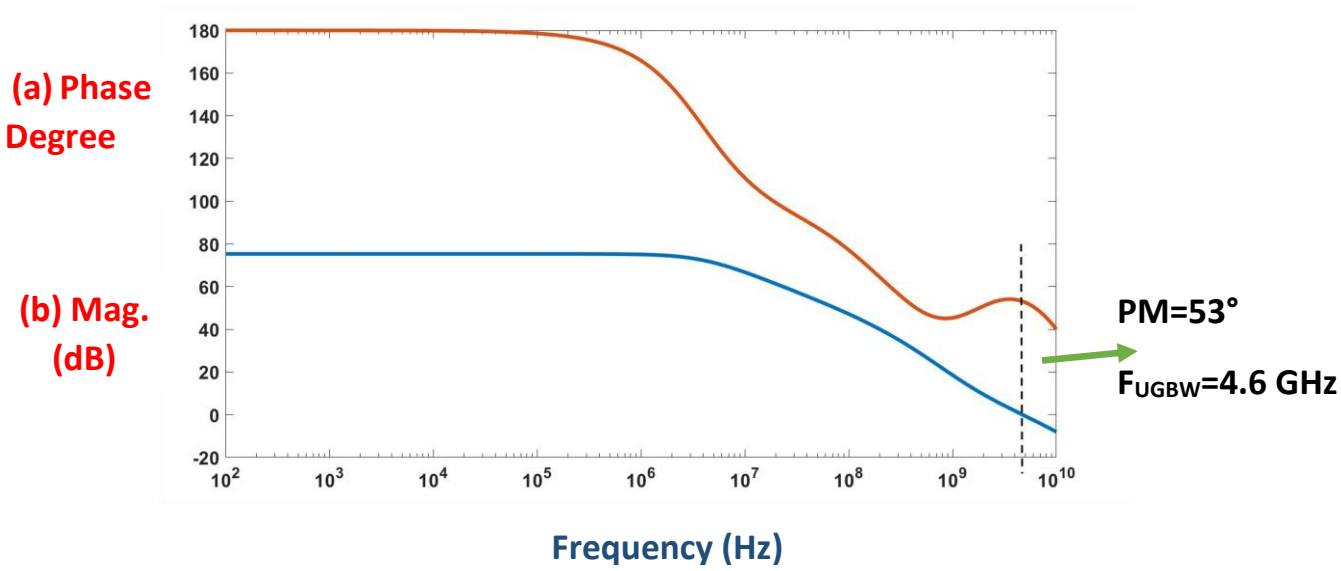

Fig. 8 Frequency response of the TIA (open loop) (a) Phase (b) Magnitude.

Another TIA's test is to evaluate the settling time of C-array in conjunction with the TIA. The settling time is defined when the differential voltage across the C-array settles within 1LSB at 10-bit accuracy. it should be less than half of the period of clock frequency with appropriate margin if the system works well.

The test-bench is shown in fig. 9. First, the left capacitors (selected by the orange are and model two C-array equivalent circuits) are charged to an initial voltage, then the switches are closed at t=1ns. The initial voltage depends on the kind of settling time we aim to do. In other words, it is intended to measure either large or small signal settling time.

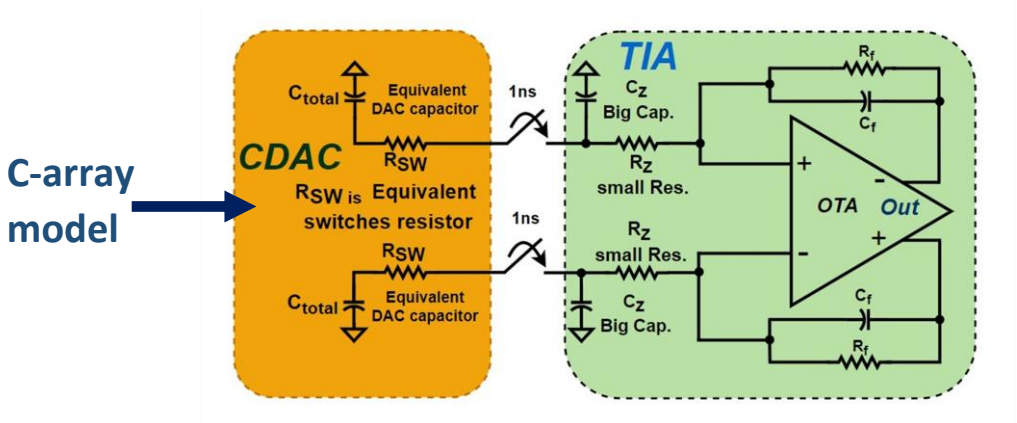

Fig. 9 Test-bench for measuring the settling-time.

Fig. 10 and Fig. 11 are shown the small signal and large signal response of the differential voltage across the C-array, respectively. The initial differential voltage across the C-array is 7mV for small signal and 700mV for the large signal test, then the settling time of the small and large signal are achieved 385ps and 364ps, respectively.

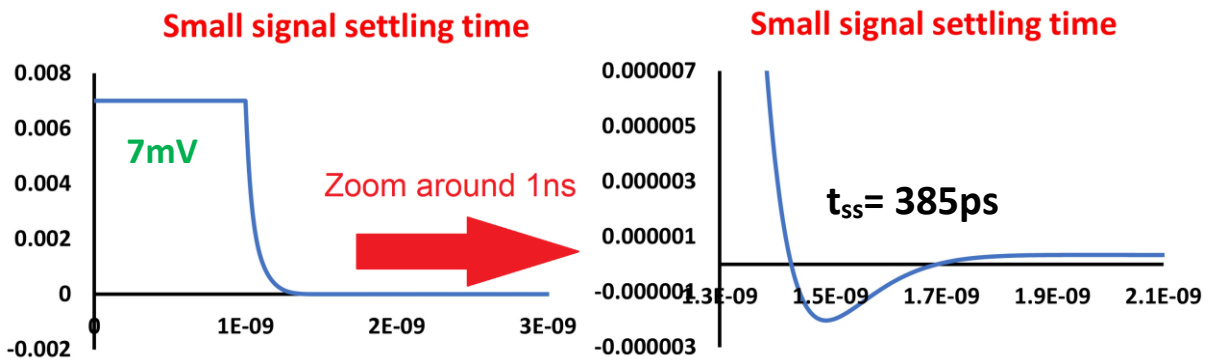

Fig. 10 Small signal response of the differential voltage across the C-array.

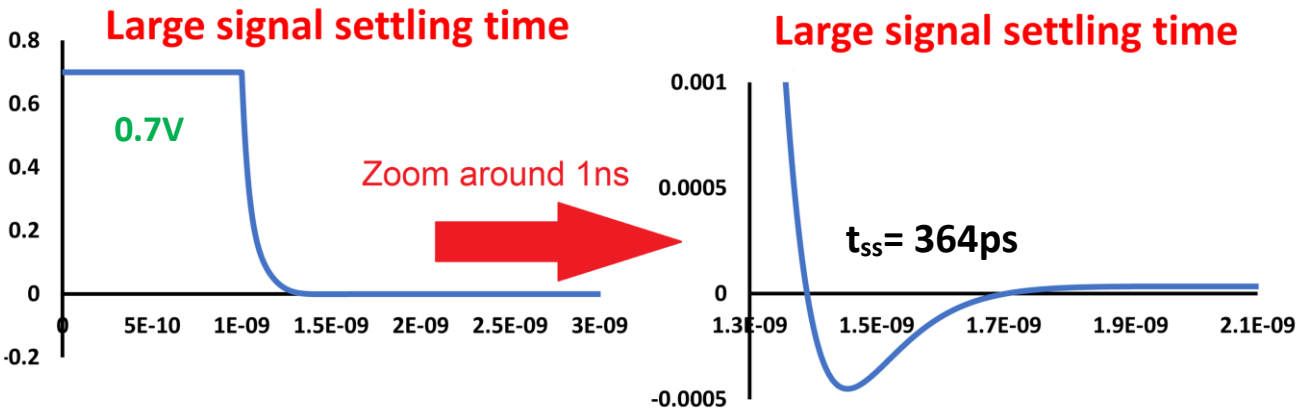

Fig. 11 Large signal response of the differential output voltage of the C-array.

3-2) CDAC/ SIC performance

The detailed information of the C-array is explained in the 1st and 2nd year report, and the 2021 PRIME article. I would like to repeat some of the important points here.

- 10-bit C-array is developed here.
- Total C-array capacitance and unit capacitance of the array are equal to 1pF and 8fF, respectively. C_{total} creates cancellation current.
- The clock frequency of each C-array is supposed to 1GHz, here.
- The supply voltage and reference of the C-array are 1V and (0.3V / 1V), respectively (they are chosen in order to obtain maximum cancellation).
- There is trade-off between the TIA's output swing and amount of cancellation because common mode voltage of the C-array is 0.5V (because of using the low-voltage switches) and analog common mode voltage (V_{CMA}= V_{ddA}/2) are different. If V_{CMA} become close to the 0.5V the cancellation will increase but the swing will decrease. Otherwise, the sub-blocks' designs are changed.

3-2-A) a stand-alone CDAC simulation

In this mode, the block works as *a standalone CDAC* with a 1GHz clock frequency. The fig. 12 shows the used test-bench with the following assumptions.

- In fig.12, switch 1 and switch 2 are open and periodically become close/open, respectively.
- An ideal 1st order low-pass filter is located after the TIA in order to verify the oversampling effects of the CDAC.
- The BIST part generate a 10-bit stream of a digitized sinusoidal waveform with the base-band frequency (chosen according to the coherent sampling) and amplitude of 10.7421875MHz and 1LSB less than full scale, respectively.

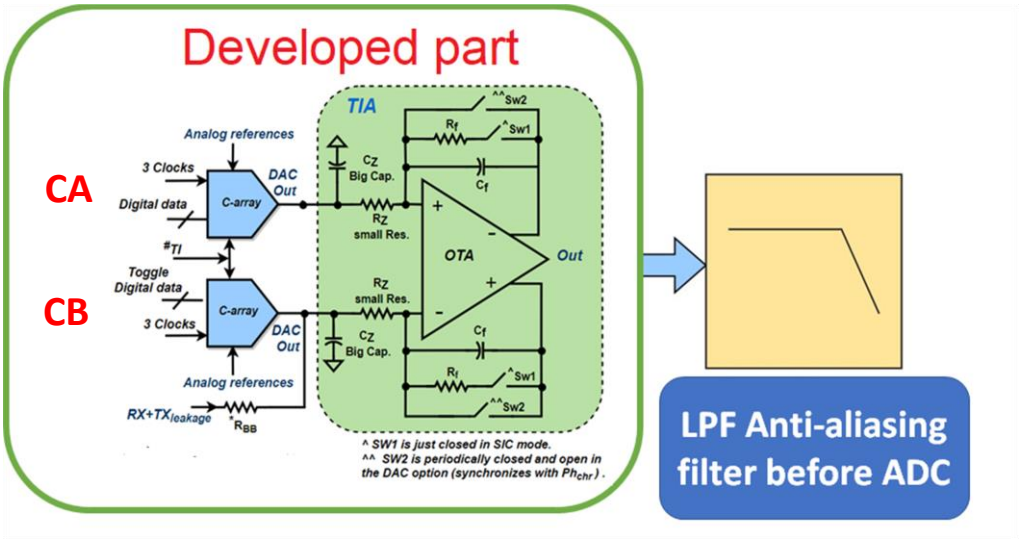

Fig. 12 Test-bench for characterizing the CDAC.

The result of the simulation of before and after 1st oder ideal LPF is reported below.

Table III the one CDAC dynamic performance (F_{BB}~10.7MHz & $Amp._{BB}$~ full scale).

	ENOB (bit)	SINAD (dB)	SFDR (dBc)	THD (dB)	Signal power (dB)
After TIA	9.25	57.5	64	-65	-16.4
After ideal LPF	10.75	68	69	-70.5	-16.8

3-2-B) Two tone test simulation

The test-bench of this test is like the fig. 12. There are some differences in the simulation assumptions as follows. The result of the two-tone simulation is reported in the fig. 13

- Two C-array works with the same clock frequency.
- CDAC-A and CDAC-B works with the same amplitude equal the full scale.

- The base-band frequency of the CDAC-A and CDAC-B are equal to 10.7421875M and 8.7890625MHz, respectively.

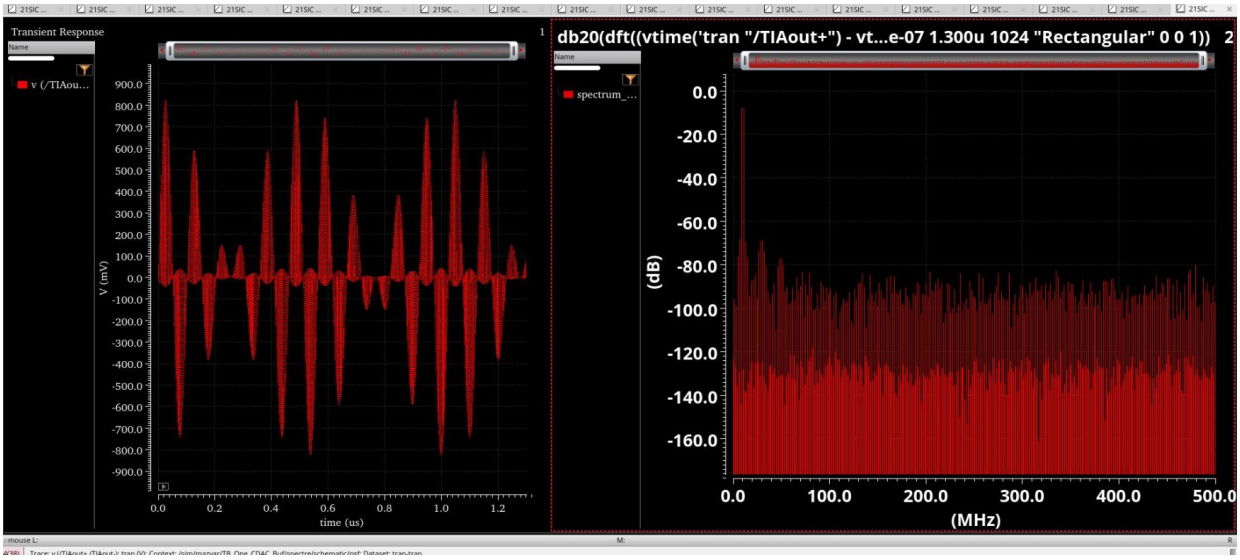

Fig. 13 Two tone test.

3-2-C) SIC simulation

In this mode, the block works in SIC mode. CADC-A/B works in the time-inter-leaved (TI) mode with a 1GHz clock frequency to create 2GHz self-interference cancellation (two times of the mixer frequency in order to avoid mutual interference in SIC mode, equal 2GHz).

. The fig. 14 shows test-bench of this test with the following assumptions.

- Switch 1 and switch 2 are permanently close and open in this test.
- The BIST part generate a 10-bit stream of a digitized sinusoidal waveform with the base-band frequency (chosen according to the coherent sampling) and amplitude of 10.7421875MHz and 1LSB less than full scale, respectively.
- A Sin generator signal with the same base-band frequency is connected between BB+ and BB- *as a TX leakage signal.*
- The resistance of R_{BB} and peak voltage of TX voltage source (V_{BB}) equal to 2KΩ and 2.6V, respectively. It is equivalent to 0.65mA (peak) current.

The simulation's result of SIC mode is reported in the table IV. The most important parameter of the table III is $SNDR_{equv.}$ (the last column and defined as SNDR after cancellation referred to the signal before cancellation). 60.9dB is close to our target.

Table IV the SIC mode dynamic performance.

	TX In. (V_p)	Output (dBV)	Cancl. (dB)	SNR (dB)	SFDR (dB)	SFDR (dBc)	THD (dB)	$SNDR_{equv.}$ (dB)
TIA output	2.6	-41.1	46.4	15.6	14.5	21.3	-20.1	60.9

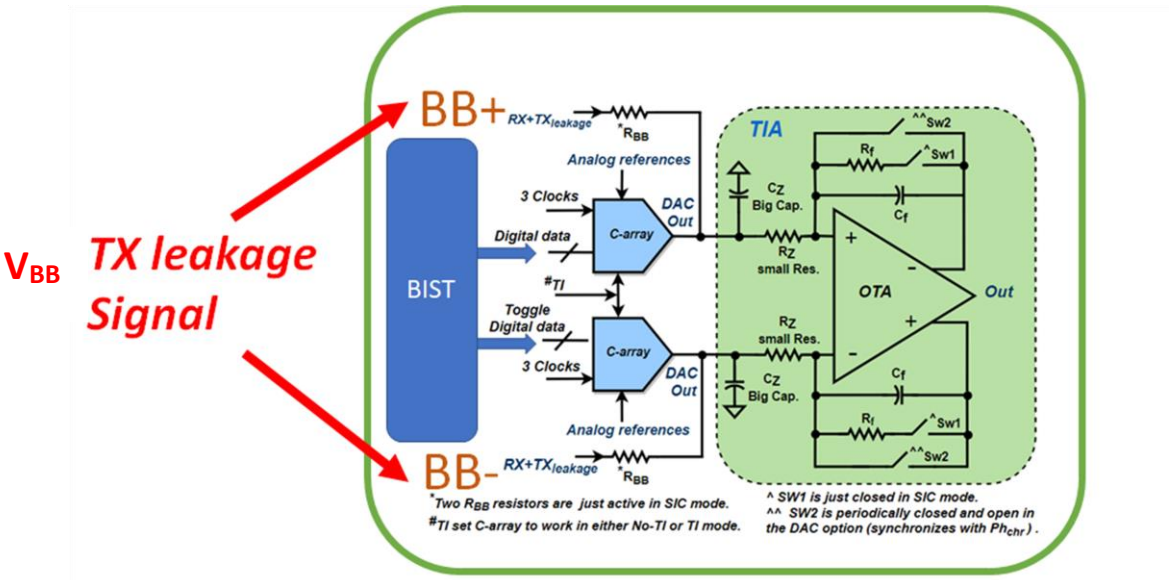

Fig. 14. Test-bench of simulation of SIC mode.

3-3) Buffer performance

The buffer is located between outputs of the TIA and the outside of the chip. Its frequency response should not degrade the CDAC/SIC performance. It is a class-A source follower. You could see its frequency response in the fig. 15.

- The gain of buffer is constant (-1.25dB) up to 100MHz and it just drop less than 1.5dB until 1GHz. It shows the buffer works well in our design.
- The phase drop -3.9° and -34° on 100MHz and 1GHz, respectively.
- When the voltage source with the peak voltage equal to the maximum swing of the TIA is connected to the buffer, the SFDR is obtained 75.5 dBc.

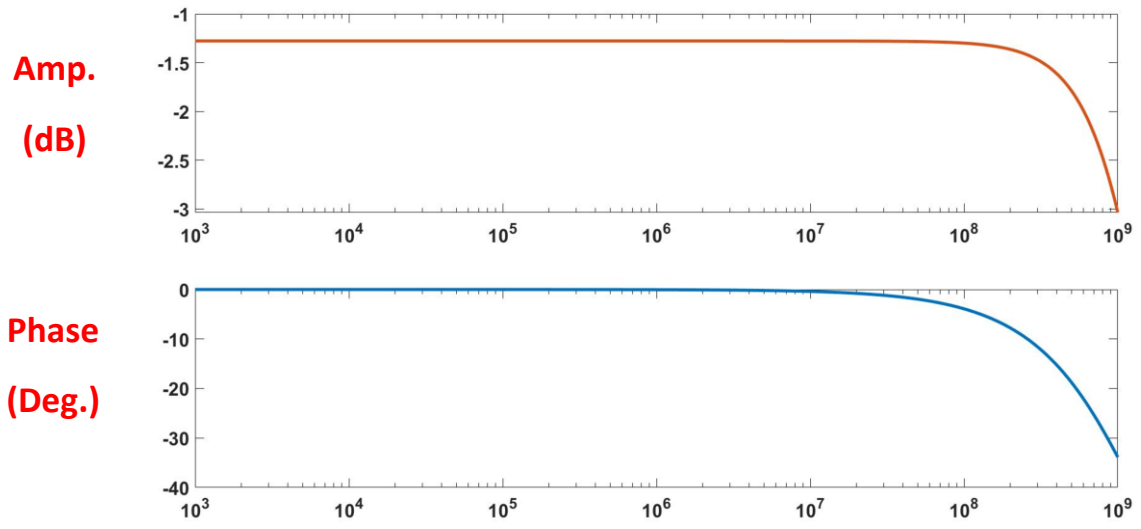

Fig. 15 Frequency response of the output buffer (a) Amplitude (b) Phase

There is additional explanation about digital part. BIST and controller are developed by HDL and manually, respectively.

- As we see in fig. 16, the chip divides up to two sections. The BIST is located the bottom of the chip.
- The BIST part could be programmed by the serial interface.
- The input bits of the C-array and some initial programing bits (like mode select) comes from the bottom part of fig. 16.
- The high-frequency clock of BIST section comes from the manually deign part (top of the chip), hence, there is delay between the clock and the generated data (output data of BIST)- around 100 to 130ps. It is shown below.

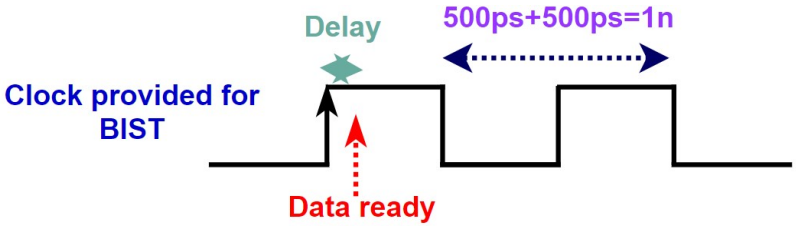

Fig. 17 generated clock

- A 7-level programmable delay circuitry is designed to compensate this delay. You could see the amount of the variable delay in the table V. For example, if $b_0b_1b_2$ sets to 111 the new clock is feed to the C-array with around 160ps delay with respect to the original clock.

Table V programmable delay for the clock.

	b0	b1	b2
Delay	~20ps	~40ps	~100ps

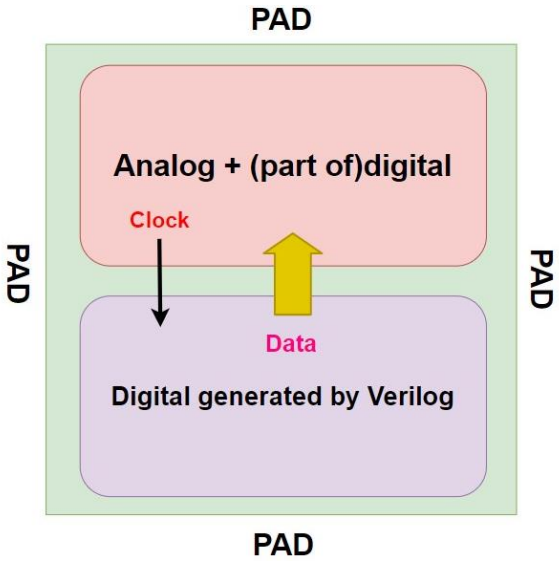

Fig. 16 The whole chip

The total chip area is 1110um by 1110um along with 40pins as shown in fig. 16.

- The bottom part of the chip is developed by HDL and used 20-pins
- The top part is manually designed and occupied and used half of the area of the chip and 20-pins, respectively.

The floor planning of the manually designed section is shown in fig. 17 above.

❖ There is not only direct connection between the analog and digital ground inside of the chip but also, they are located far from each other in order to avoid noise of high-frequency digital circuits couples to the sensitive analog parts.

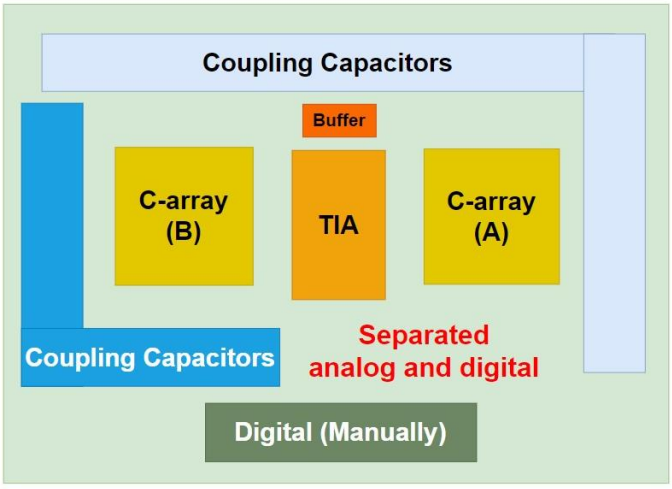

Fig. 17 The floor planning of the manually drawn section.

The layout of C-array is shown in fig. 18. There are just C_U, $2*C_U$, $4*C_U$, in the array, so the design become relatively less sensitive to symmetric and linear and gradient oxide process and drawing the layout is simpler.

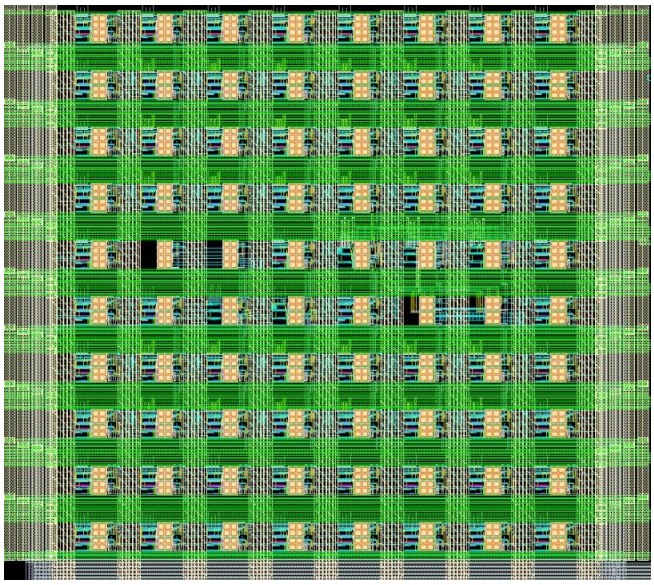

Fig. 18 Layout of the C-array

The manually developed circuits is shown in fig. 19(a), without showing automatically generate digital circuit part.

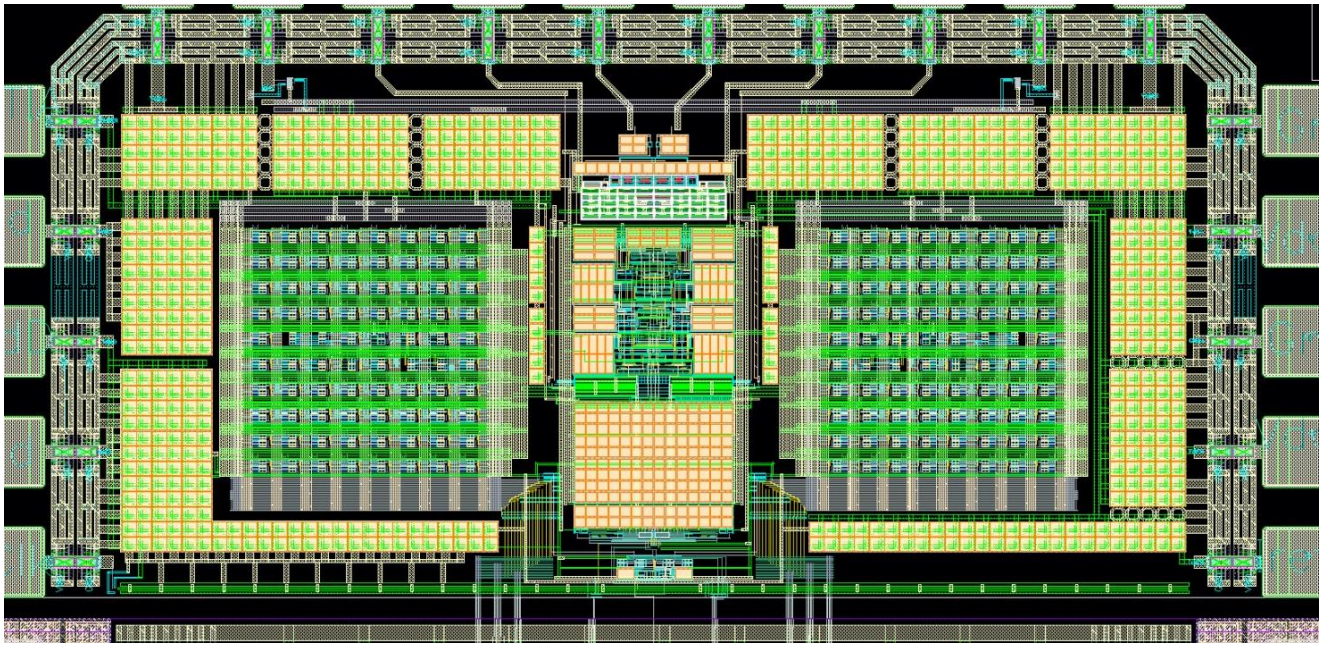

Fig. 19(a) The layout of manually designed section.

- The location of different parts of the design is shown in fig. 19(b) with more details.
- The core of the chip is surrounded by Coupling capacitors. The supply and references first go to the coupling caps, then are connected to the sub-blocks.

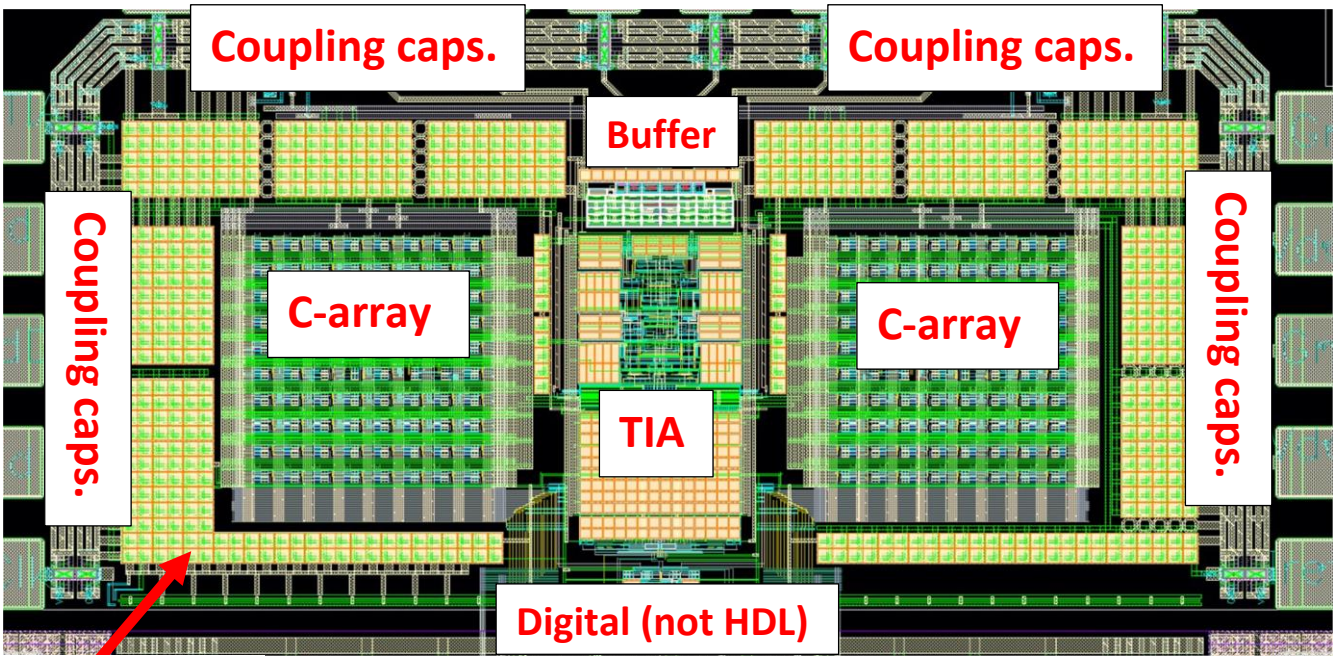

Fig. 19(b) The layout of manually designed section.

The whole layout of the chip is shown in fig. 20 including manual and automatic design's layout.

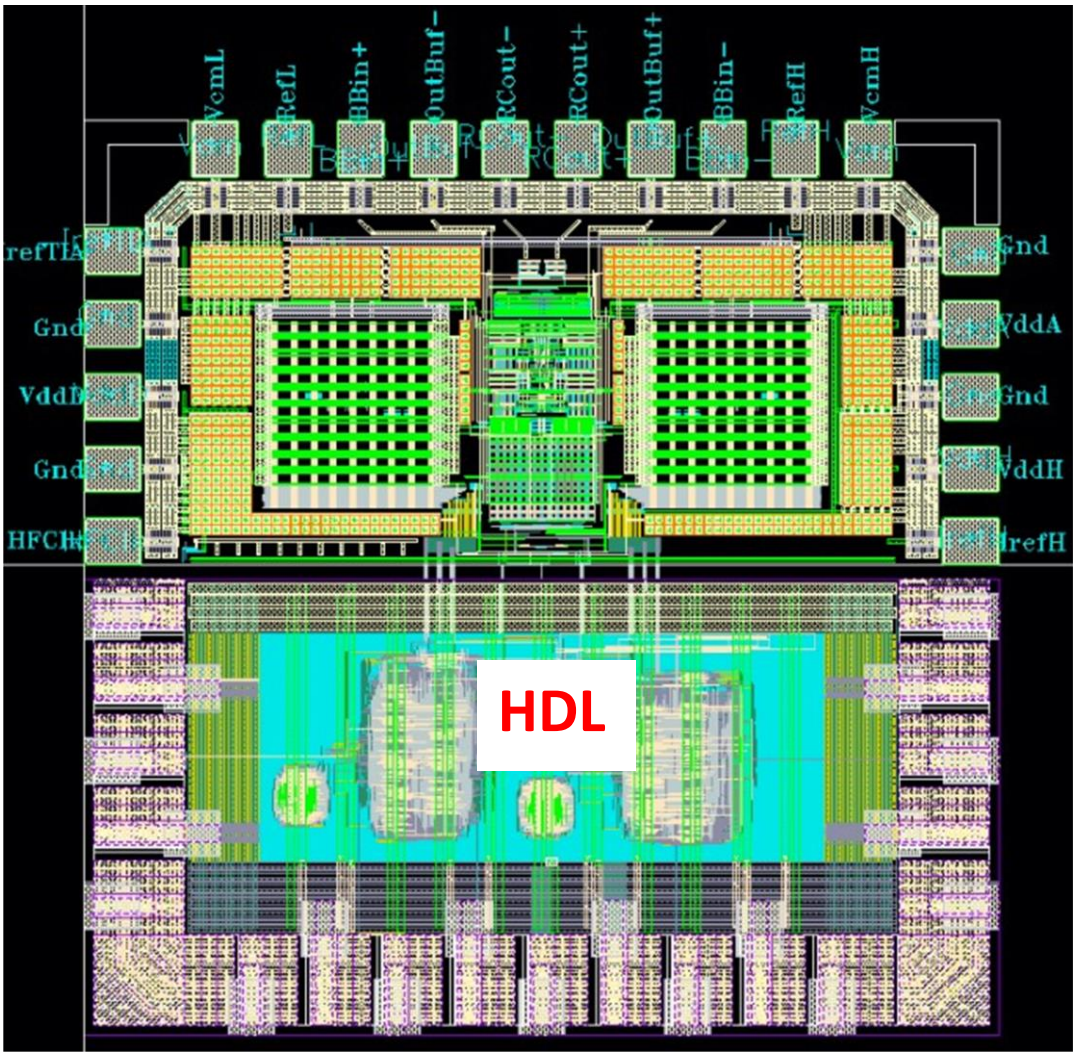

Fig. 20 The layout of the chip.

5- References

[1] D. Montanari et al., "An FDD Wireless Diversity Receiver with Transmitter Leakage Cancellation in Transmit and Receive Bands," IEEE JSSC, vol. 53, no. 7, pp. 1945-1959, July 2018.

[2] A. H. Chang, H. S. Lee, and D. Boning, "A 12b 50MS/s 2.1mW SAR ADC with redundancy and digital background calibration," IEEE ESSCIRC, pp. 109–112, Sept. 2013.

[3] C. Lin and K. Bult, "A 10-b, 500-Msample/s CMOS DAC in 0.6 mm," IEEE J. Solid-State Circuits, vol. 33, pp. 1948–1958, Dec. 1998.