UNIVERSITA' DI PAVIA

DEPARTMENT OF ELECTRICAL, COMPUTER
AND BIOMEDICAL ENGINEERING

Ph.D. Course in Microelectronics

XXXVII CYCLE

First Year Activity Report

Frequency Multiplier by four at 80 GHz (CMOS)

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Academic Year 2021-2022

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Introduction

The research activity of this first year is to implement a frequency multiplier by four at 80 GHz. Why to use a frequency multiplier. In general, DCO with high output frequency can be challenging to be designed. The phase noise increases with frequency. A possible solution for that problem could be that of using a low output frequency oscillator followed by a frequency multiplier.

The present *frequency multiplier* adopts an approach based on selection of the harmonic component generated by a nonlinear active device. By exploiting the nonlinearity of an active device, it is possible to convert an input frequency, f_{in}, into an output frequency $f_{out} = n \cdot f_{in}$ (with "n" integer number).

The easiest way to implement a frequency doubler is with transistors biased at a low conduction angle to generate a strong second harmonic of the input frequency, and by using a pair of devices driven by balanced signals (the push–push configuration). The fundamental component and all odd-order harmonics are suppressed thanks to matching, without requiring highly selective filters. The majority of frequency doublers with output signal near or above 100 GHz require high input power (Pin), typically greater than the output power (Pout). The resulting negative power-added efficiency (PAE), given by PAE = (Pout −Pin)/PDC (being PDC be the power consumption), demands a driving stage or an output amplifier to increase the overall conversion gain and output power, which increases power dissipation.

The design will be carried out using TSMC 28nm HPC technology (CMOS).

In the following sections the design and characterization of the multiplier implemented during the first tape out will be described first, followed by the design of the multiplier implemented during the second tape out.

1 Multiplier Target Specifications

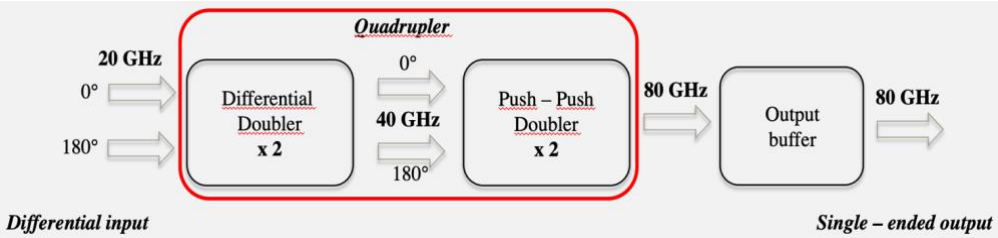
The frequency multiplier required in this project is a **Frequency Quadrupler** with 76 – 81 GHz output frequency range. The key performance targets are listed below:

- Input frequency: around 20 GHz
- Output frequency range: 76-81 GHz
- Output power: above 0 dBm
- Power consumption: below 40 mW

2 First tape-out

2.1 Block diagram

The frequency multiplier has a differential input at the frequency of 20 GHz and a single ended output at the frequency of 80 GHz. It is implemented by cascading two doublers: 20 GHz → 40 GHz and 40 GHz → 80 GHz. The last stage is an output buffer that allows to load the quadrupler output with 50 Ω and introduce the necessary gain to increase the output power. The first stage is a *differential doubler* (differential input and output) whereas the second one is a *push – push doubler* (differential input, single ended output).



2.2 Architecture and schematic of the frequency quadrupler

The frequency quadrupler is composed of two frequency doublers, both based on simple push-push configurations, but with different topologies. The topology of the first doubler is a differential push – push configuration with PMOS and NMOS connected together by a differential inductor, as shown in Fig.2. The inductor resonates the total parasitic capacitances of the transistors at 40 GHz.
The two transistors are biased at the edge of class-C, which means with a gate-source voltage, V_{GS}, just below the threshold voltage, V_{th}. This ensures high current efficiency, i.e. high second harmonic component of the current with respect to the average current, thanks to the nonlinear characteristic of the MOS transistor. An LC load resonator placed at the drains selects the second harmonic. A control loop sets the bias of the PMOS pair in order to fix the inductor center tap

voltage to half the V_{DD}. The big capacitor C_{big} in Fig.2 is used to filter the current signal due the mismatch between the current generated by the PMOS and NMOS pairs.

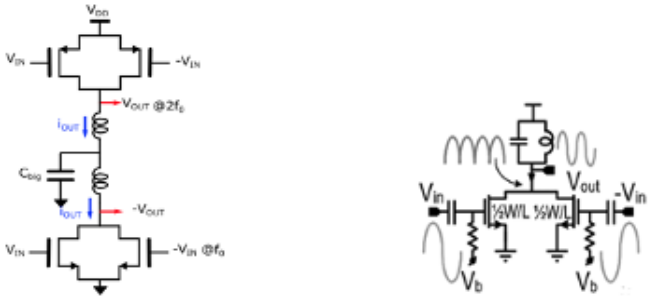


Figure 1 - 1st doubler: PMOS and NMOS push push doubler and 2nd doubler: push-push pair

The schematic used for simulations is reported below

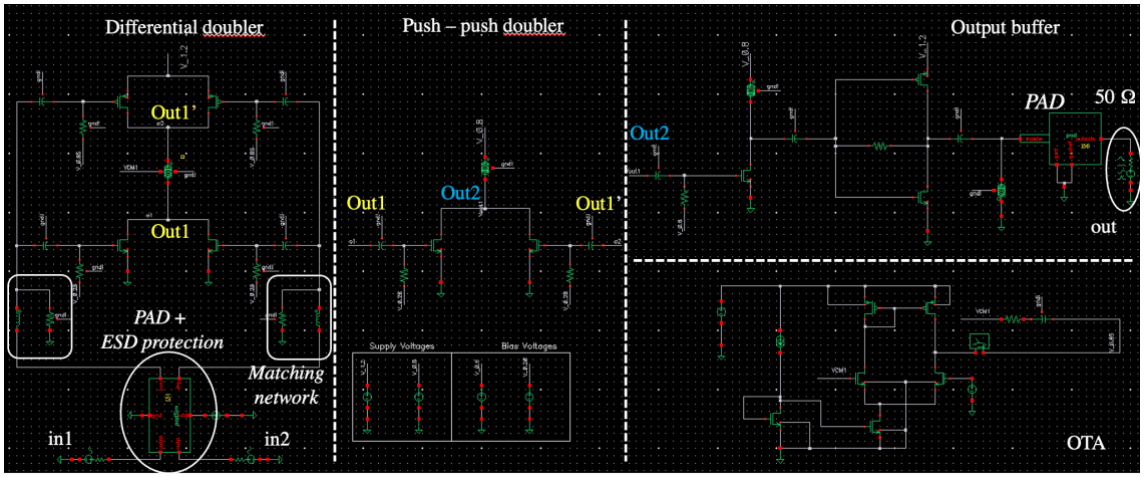


Figure 2 - Multiplier schematic

In the schematic is also shown the output buffer which is used to increase the gain of the overall circuit. This latter is the cascade of a tuned common source amplifier and a push-pull amplifier self-biased by a big resistor. A transimpedance amplifier (OTA) is used to self-bias the PMOS transistors of the differential doubler. It uses the Common Mode Feedback to fix the bias voltage at the gate of the transistors and the DC voltage at the inductor tap to half supply voltage.

2.3 Layout

The following figure is the layout of the quadrupler

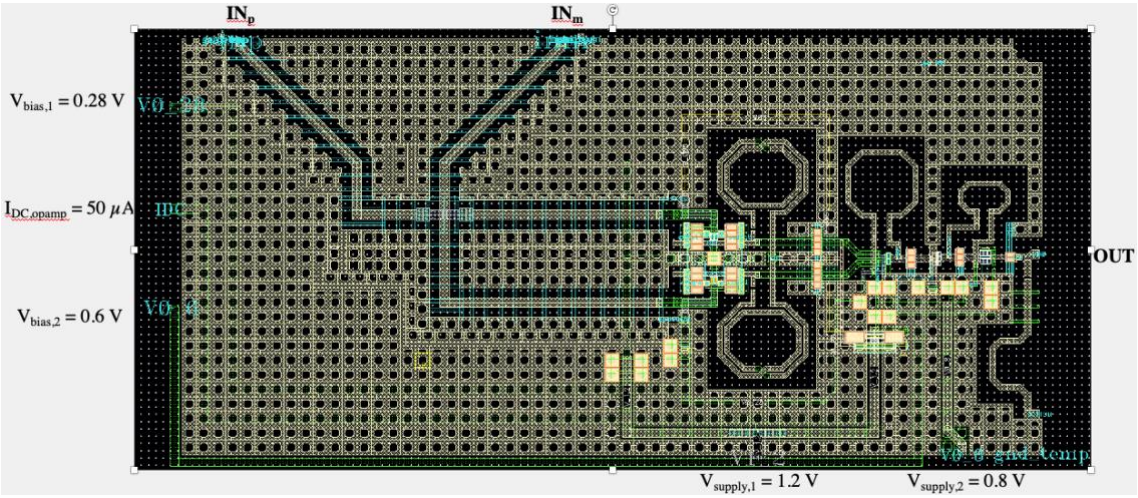


Figure 3 - Quadrupler layout

It is possible to see the ground plane that covers most of the chip. On the left side, there are three lines for biasing. On the bottom, there are the two supply voltages: 0.8V and 1.2V. On the right side, there is the single ended output and, on the top, the differential input. The length and width are 0.6 mm and 0.3 mm respectively.

2.4 Simulated and measured results

The evaluation of the output power vs input frequency is reported below

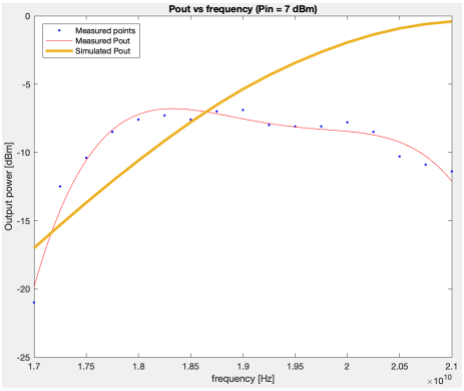


Figure 4 - output power vs input frequency

The yellow line highlights the simulated output power while the other curve is representative of the measurement points.
The peak output power is less than expected and remains relatively flat from 72 to 81 GHz (18 to 20.5 GHz input frequency).
Tables regarding the simulation and measurement results are shown here

Parameters	Target Spec	Post-layout sim	Measurements
P_i (Single-ended)	-	7 dBm	7 dBm

P_o (in 76-81 GHz BW)	0 dBm	*≃ -2 dBm*	*≃ -8 dBm*
P_{DC}	< 40 mW	13.8 mW	≃ 12.9 mW
FHR	-	59 dB	-
DC – RF efficiency η	-	4.6 %	1.2 %
Conversion Gain (CG)	-	-12 dB	-18 dB

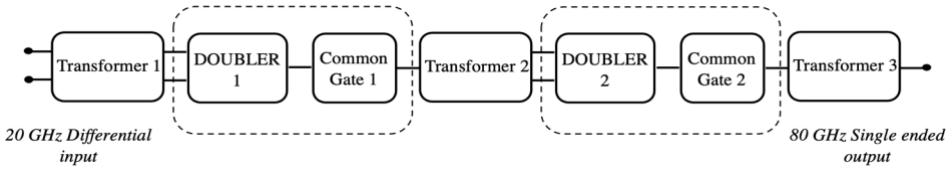
FHR (fundamental harmonic rejection) represents how much the fundamental component is rejected with respect to the second harmonic at the output. The efficiency expresses the ratio between output power, P_o, and DC power consumption. The conversion gain (CG) is expressed as the ratio between output power at 80 GHz and differential input power at 20 GHz.
From the table, it sees that the measured performances are not perfectly in line with simulations. For this reason, a new design has been performed.

3 Second tape-out

In the second tape-out a new design concept has been developed with the aim of resolving some of the issues that were encountered during the first design, namely the limited gain, bandwidth and output power.

3.1 Block diagram

The quadrupler is composed of two doublers, three transformers, used to convert single ended to differential signal and to realize a broadband matching and two common gate amplifiers to increase the output voltage needed to drive the cascaded stage.



3.2 Architecture and schematic of the frequency quadrupler

The main used block in the quadrupler is the *push – push doubler*. This is the classical topology used to exploit the nonlinearity of an active device to generate, at the output, the desired second harmonic component of the input frequency. The MOS transistor is, then, driven into compression such that the drain current is rich with even harmonic components of the input signal. A resonant load selects the desired one.
For maximum conversion efficiency the device conduction angle must be chosen to maximize the second harmonic of the current.

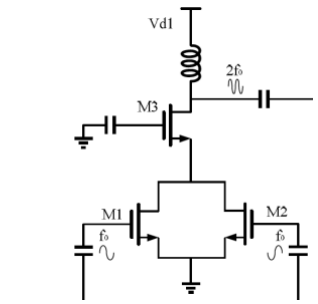


Figure 5 - Cascode frequency doubler

The topology used to realize the doubler is shown in Fig. 5. It is a push-push pair cascaded by a common gate amplifier. This latter can be exploited to improve the overall conversion gain. This amplifier senses the input current, which is generated by the doubler, and produces an output voltage which is big enough to drive another frequency doubler having a similar topology.
The schematic used for simulations is reported below

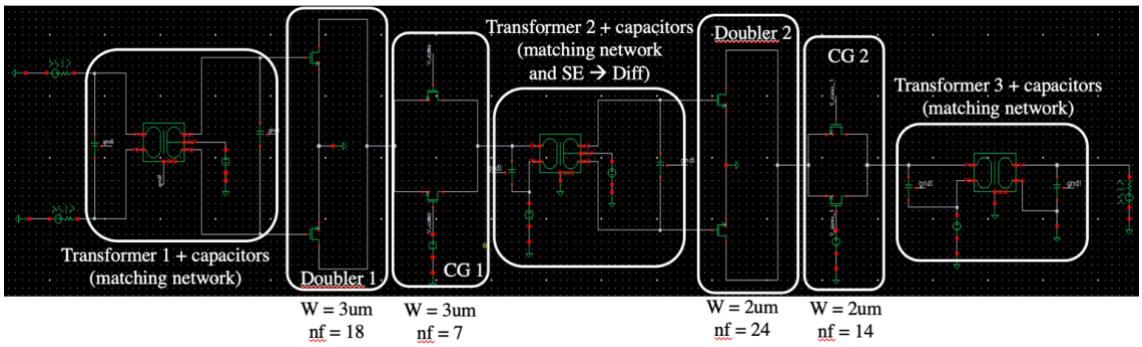


Figure 6 - Quadrupler schematic

It is possible to see in the schematic the different stages mentioned before and the transformers placed in the middle of each stage. These latter are used to realize a broadband matching by varying the coupling coefficient properly. This can be performed by horizontally shifting the primary and the secondary winding one each other.

3.3 Layout

The following figure reports the layout of the new design

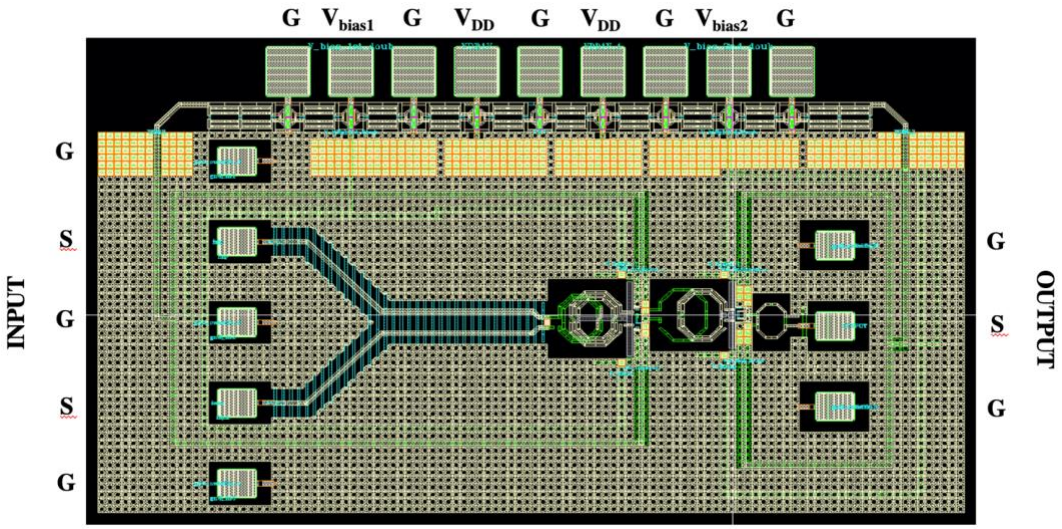


Figure 7 - Quadrupler layout

It is possible to see the ground plane that covers most of the chip. On the left side, GSGSG differential input pads can be seen. On the right side, there are GSG single-ended output pads. On the top, pads for bias and supply voltages are reported. The core of the multiplier is in center of the chip. The length and width are 1 mm and 0.63 mm respectively.

3.4 Simulated post layout results

In this section post layout results will be reported. In particular, the evaluation of the output power as a function of input frequency for a single-ended input power level of 0 dBm.

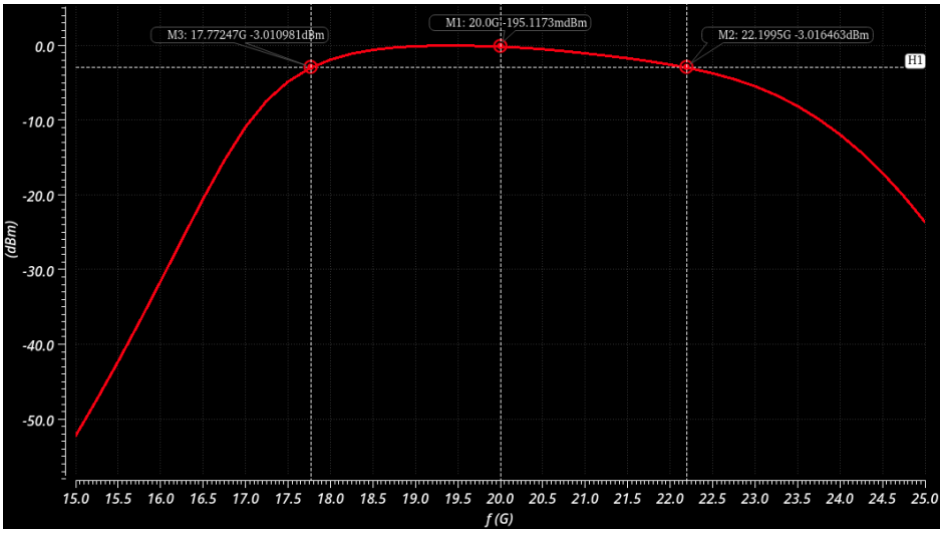


Figure 8 - Output power vs input frequency

The output power at 80 GHz is around 0 dBm (target value). The power remains almost constant in the input frequency range 17.7 – 22.2 GHz (70.8 – 88.8 GHz output frequency range), therefore, -3 dB bandwidth is around 18 GHz.

Assuming input signal amplitude and frequency fixed, the post layout simulations results are summarized in the table.

THE OVERALL CIRCUIT (50 Ω LOADED)	
V_{DC}	1 V
P_i (Single-ended) (differential)	0 dBm 3 dBm
f_{in}	20 GHz
f_{out}	80 GHz ($BW_{-3dB} \simeq 18\ GHz$)
P_o	$\simeq 0\ dBm$
I_{DC}	10.2 + 13 = 23.2 mA
P_{DC}	10.2 + 13 = 23.2 mW
FHR	88 dB
Conversion Gain (CG)	-3 dB
DC – RF efficiency η	4.3 %

Better results have been achieved with the new design of the quadrupler.
Chip measurements will be the plan in the future.

Comparison table

In this chapter post layout simulations of the first and second tape-out are compared with the target specifications.
Assumptions: input frequency 20 GHz, output frequency 80 GHz

Parameters	**Target Spec**	**1st TAPE – OUT**	**2nd TAPE – OUT**
V_{DC}	-	1.2 V and 0.8 V	1 V
P_i (Single-ended)	-	7 dBm	0 dBm
P_o	0 dBm	$\simeq -2\ dBm$	$\simeq 0\ dBm$
P_{DC}	< 40 mW	13.8 mW	23.2 mW
FHR	-	59 dB	88 dB
DC – RF efficiency η	-	4.6 %	4.3 %
Conversion Gain (CG)	-	- 12 dB	- 3 dB

In conclusion, seen the post layout simulations, we can state that the new design is better than the old one. To perform a completely comparison, measurements are required.

Education Activities

PhD School

- *ESSCIRC WORKSHOP "Future of short reach interconnect" September 19th 2022 (1.8 CFR)*

Academic Course

- *RF Microelectronics (Andrea Mazzanti) (9 CFR)*

Seminars

- *Coherent Electro-Optical Transceivers for High-Speed Data Links, March 7th 2022 (0.2 CFR)*

- *Extremely High Frequency Integrated Circuits for emerging communication networks, March 14th 2022 (0.2 CFR)*

- *Serial Interface Architecture Evolution from "simple" USB at 500Mbps to the state-of-the-art 112Gbps, March 21st 2022 (0.2 CFR)*