UNIVERSITA' DI PAVIA

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Development and Characterization of a System in Package Short Circuit Protection for SiC Power MOSFET

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Abstract

With respect to silicon isolated-gate bipolar transistors (IGBT), silicon Carbide MOSFETs offer better performance in terms of maximum voltage and current. For similar blocking voltage and current ratings, they show higher current density, higher power density, lower conduction losses and better high temperature tolerance. On the other hand, due to their smaller active area, SiC MOSFETs show a lower thermal dissipation capability and consequently, a lower short circuit withstand time. Typical short circuit protection, such as desaturation measurement, designed originally for Si-IGBTs, senses the voltage across the device to detect the short circuit. This approach requires a long filter time in order to avoid false triggering during the turn on event of the power switch when an AC component of the drain current superimposes with the load current. This results in a detection time that is typically longer than the short circuit withstand time of the SiC MOSFET. Another possibility for detecting the short circuit event is to perform a direct measurement of the drain-source current. This is typically done either with shunt resistor or with contactless current sensors. Both methods come with their PROs and CONs, in particular the shunt resistor provides a good linear transfer function over a wide current range, but introduces extra conduction losses at system level. Conversely, the contactless approach allows for a sensing without introducing extra losses, but the usual input dynamic range of these sensors is tailored to properly sense the load current and not the much higher short circuit event. Consequently, the detection of the short circuit event is at risk due to the distortion introduced by the sensor itself.

The solution is based on a system in package architecture in which an analog front end (AFE) is responsible for both detecting and reacting to a short circuit condition happening in the SiC MOSFET that is co-packaged with it. In particular, the power switch active area is split into two parts: a main cell and a sense cell. The AFE senses the current level of the sense cell and if it overcomes a certain threshold the short circuit is detected. Therefore, the AFE starts the reaction phase by pulling the gate of the SiC switch down to an intermediate level, this transforms the short circuit event into a current controlled event and, consequently, the short circuit energy can be modulated and kept under control.

The proposed detection solution, being fully integrated into the power switch package without any extra pin, is completely transparent for the end-user and does not affect the behavior of the switch in normal operation. The proposed system in a package is composed of a power switch and an analog front end (AFE) integrated circuit. The power switch active area is split in two parts: a main cell and a sense cell. The IC senses the current level of the sense cell and if it overcomes the application level, a short circuit is detected.

AFE is connected with the power switch with 4 pins: $\mathrm{G_{in}}$,$\mathrm{G_{out}}$, $\mathrm{S_{in}}$ and $\mathrm{S_{out}}$. It does not have a dedicated supply, it must wake up very fast every time that the power switch turns on, harvesting energy from the gate signal ($\mathrm{G_{in}}$). It includes a current sense with a integrated $6.42m\Omega$ shunt resistor, this integrated approach allows to sense very fast and precisely the Sense Cell current, limiting noise and parasitic. When a short circuit is detected, the AFE drives the internal gate of the power switch. The $\mathrm{V_{gs}}$ is bring to an intermediate level, in order to limiting the dissipated energy. The result from system point of view is a SiC MOSFET able to withstand for about $4.5\mu s$ an over-current situation.

Simulation and characterization of the solution confirm the performance. The AFE wakes up in about $60ns$ every power switch tun on every with a negligible influence during normal operations. It achieves a short circuit detection in about $150ns$ in HSF conditions and in about $90ns$ in FUL conditions with very good temperature spread of $\mathrm{I_{th}}$. Resulting that the integrated AFE is able to modulate energy dissipation and make the SIC MOSFET robust against long time detection, without any permanents damage and destruction.